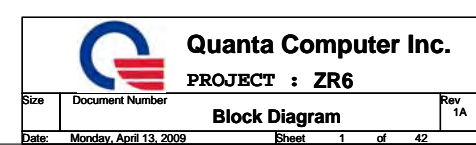
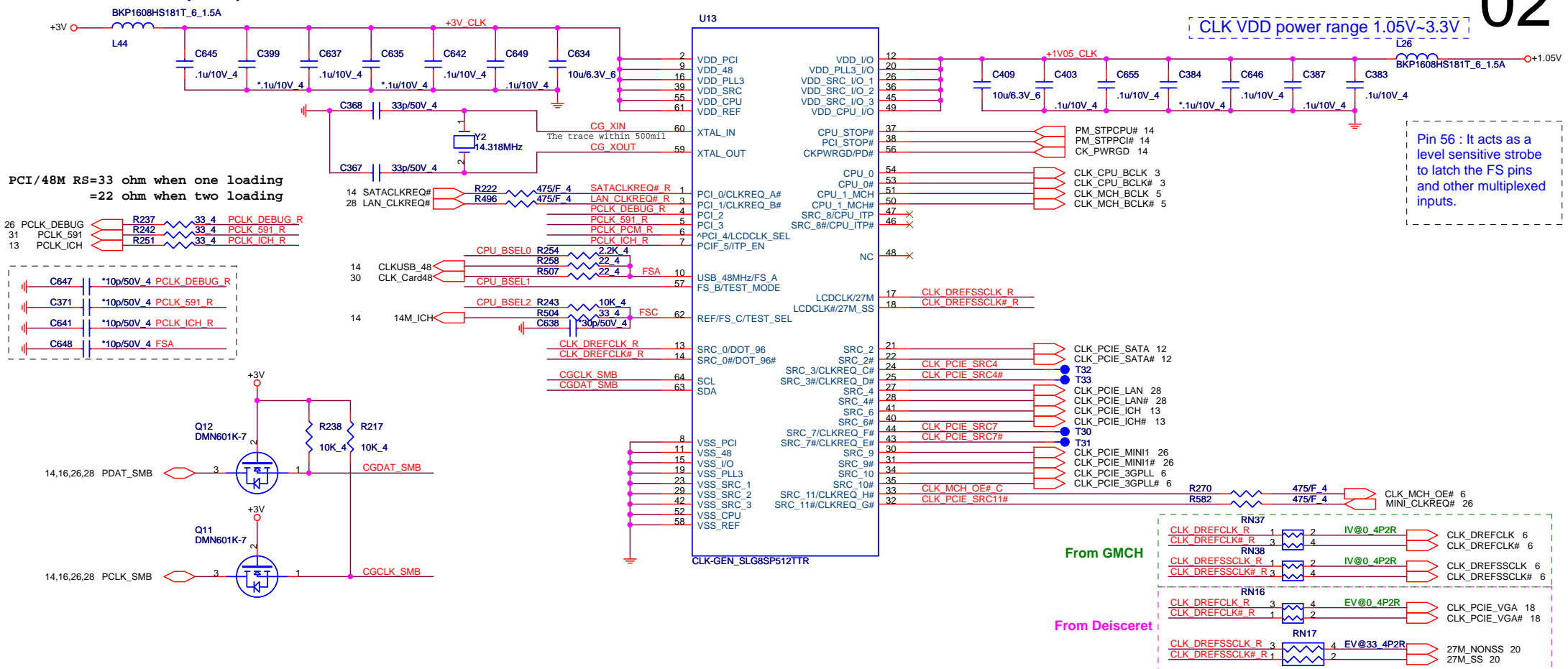


REV:C



Clock Generator (CLK)

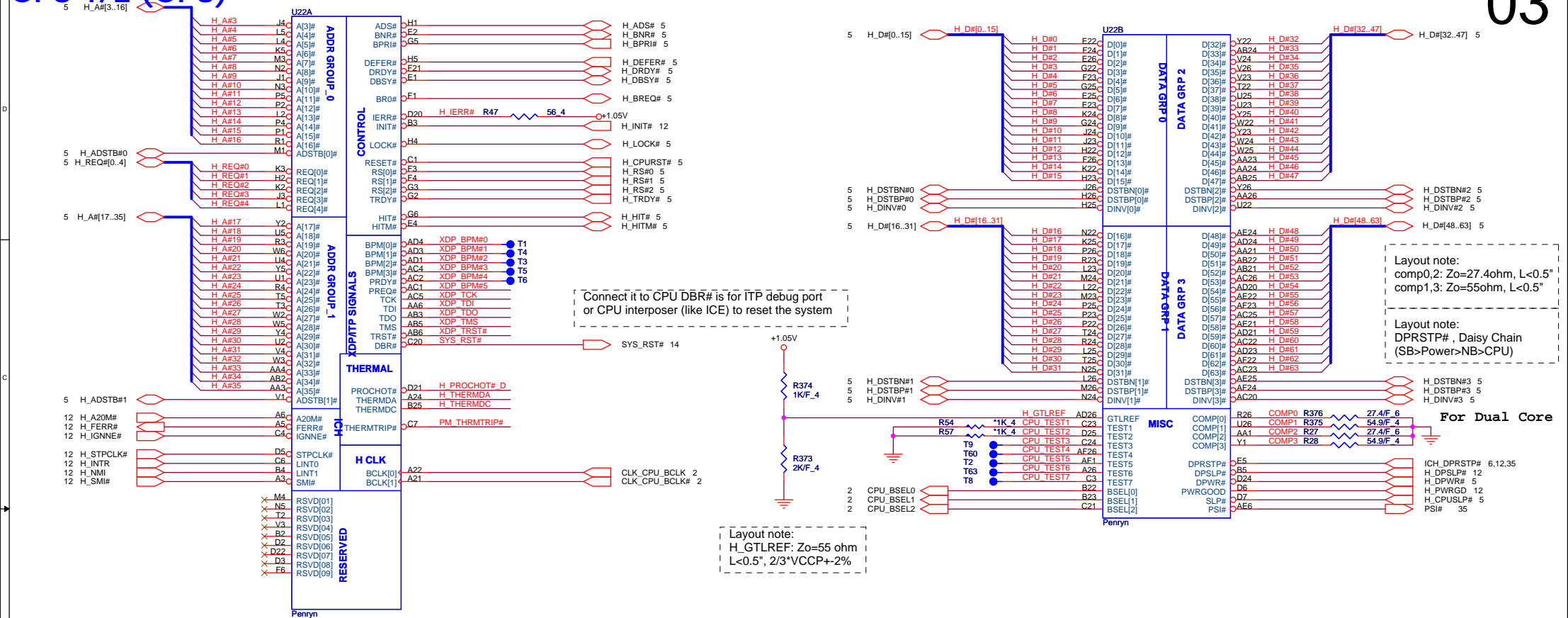


CPU Clock select

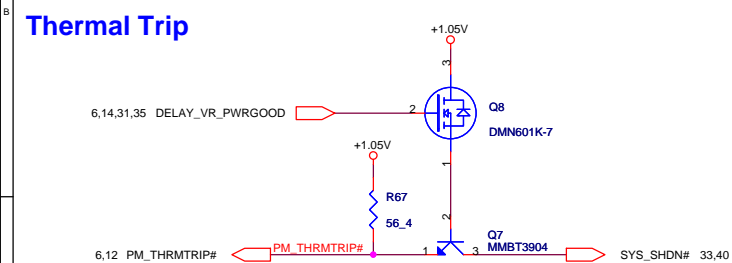
BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

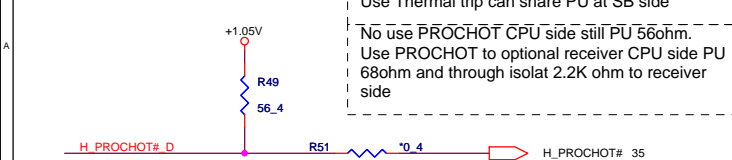
CPU 1/2 (CPU)



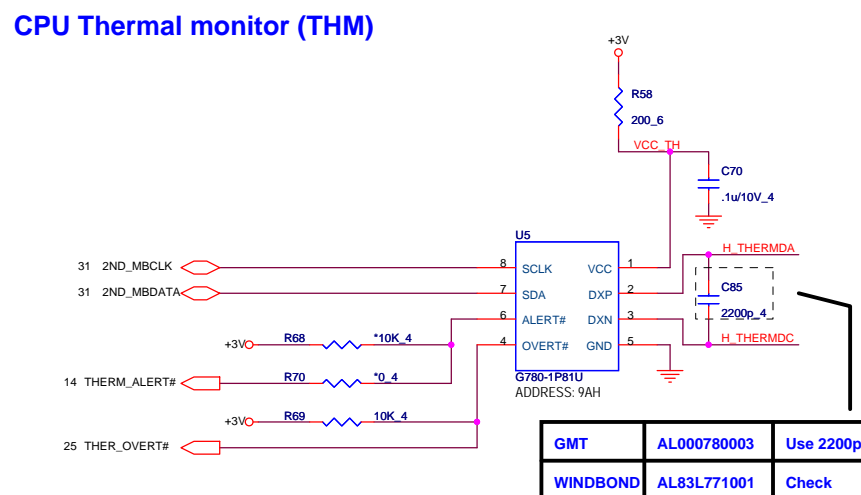
Thermal Trip



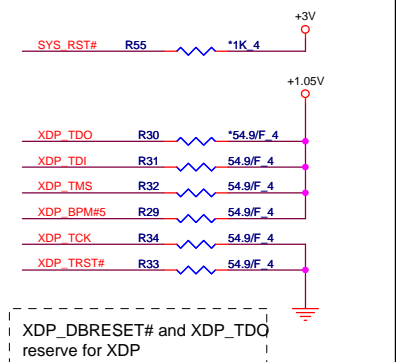
Processor hot



CPU Thermal monitor (THM)



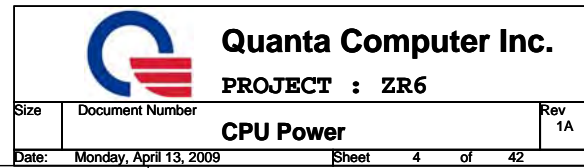
XDP PU/PD



Quanta Computer Inc.

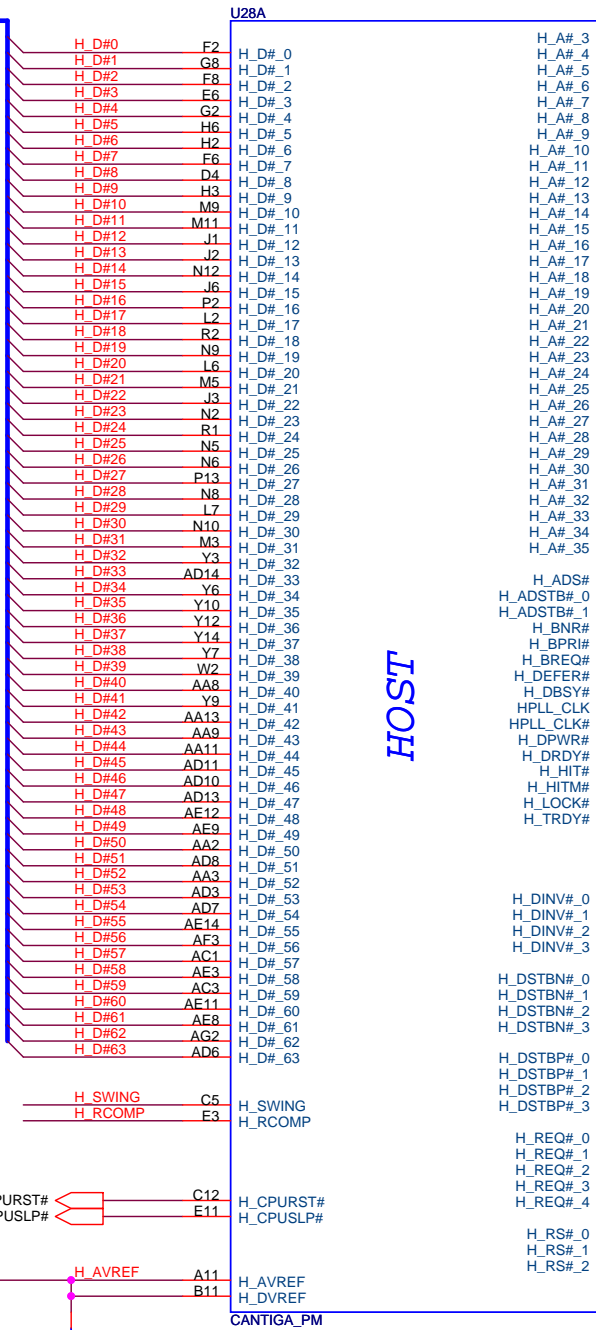
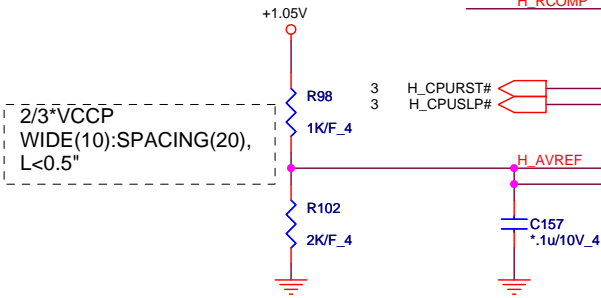
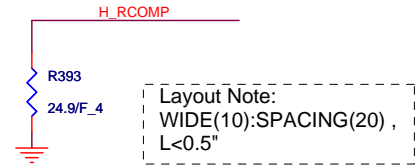
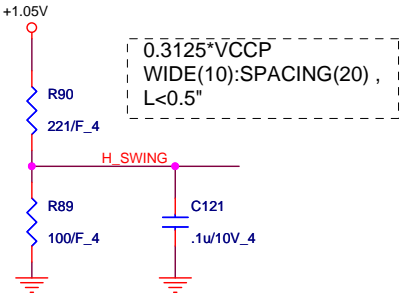
PROJECT : ZR6

04




GMCH-CANTIGA(CLG)

	QCI P/N
Intel Cantiga (G)M	AJSLB940T04
Intel Cantiga (P)M	AJSLB970T06
Intel Cantiga (G)L A1	AJSLGGM0T04



HOST



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PROJECT : ZR6

GMCH HOST

Size	Document Number	Rev 1A
Date: Monday, April 13, 2009		Sheet 5 of 42

GMCH-CANTIGA(CLG)

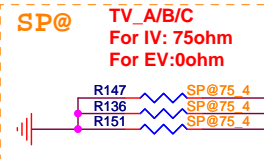
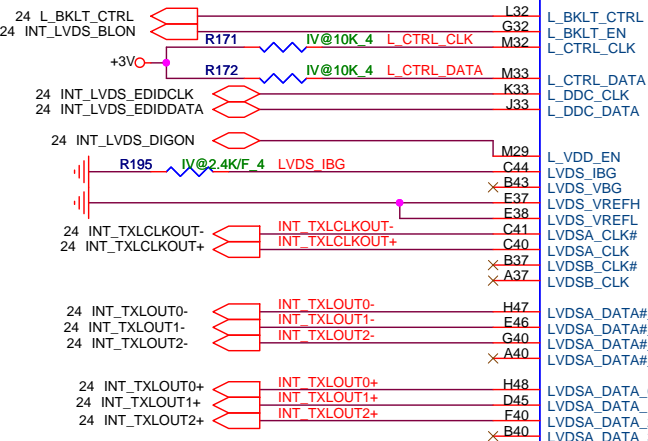
IV&EV Dis/Enable setting

If LVDS no use, all signal can NC

IV@

EV@

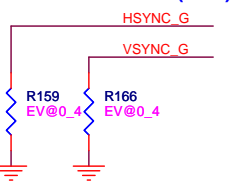
SP@



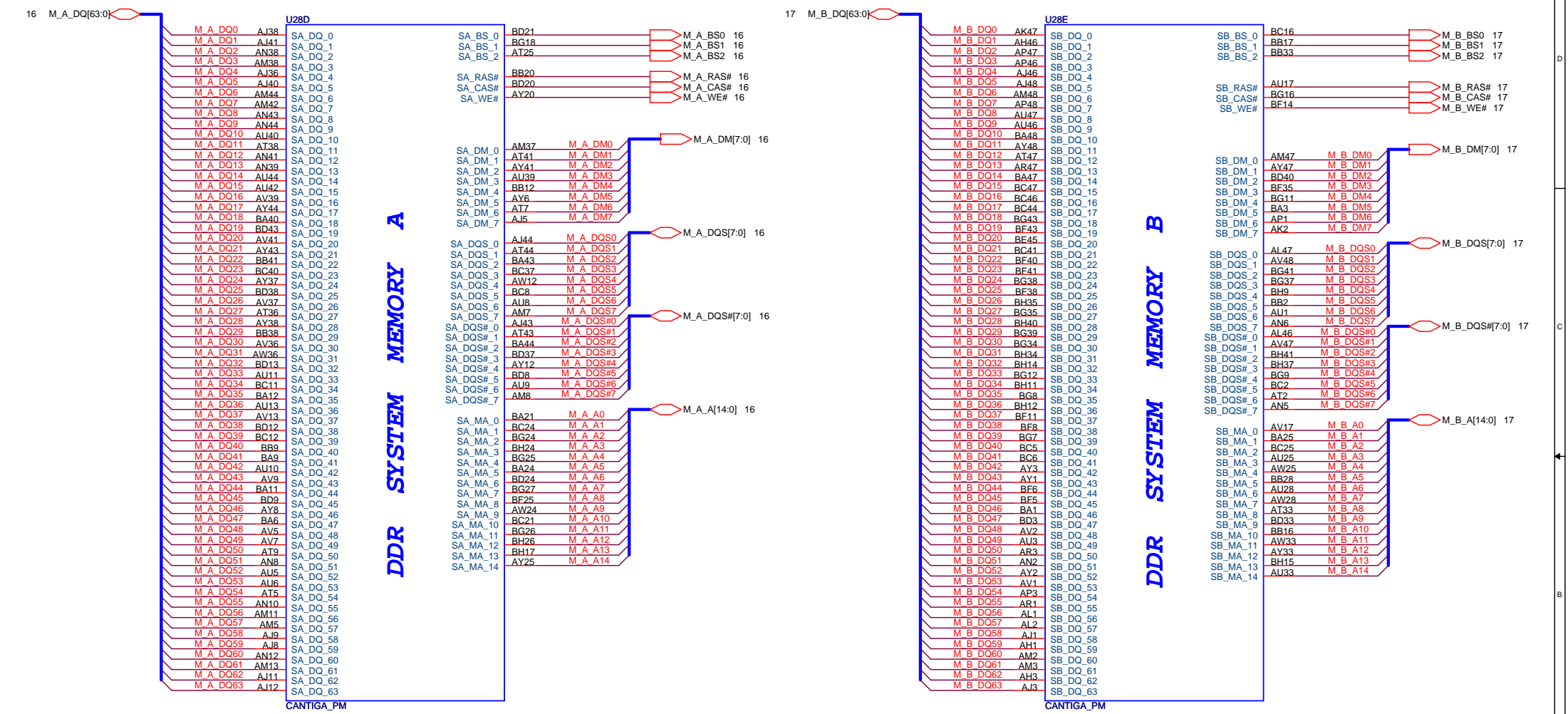
HSYNC/VSYNC serial R place close to NB

CRTIREF pull down
for IV cantiga 1.02k ohm/F


Discrete Stuffed. (CRT)



GMCH-CANTIGA(CLG)

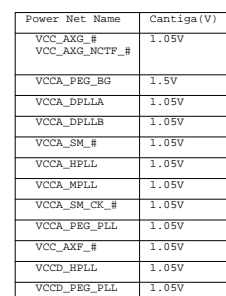


09

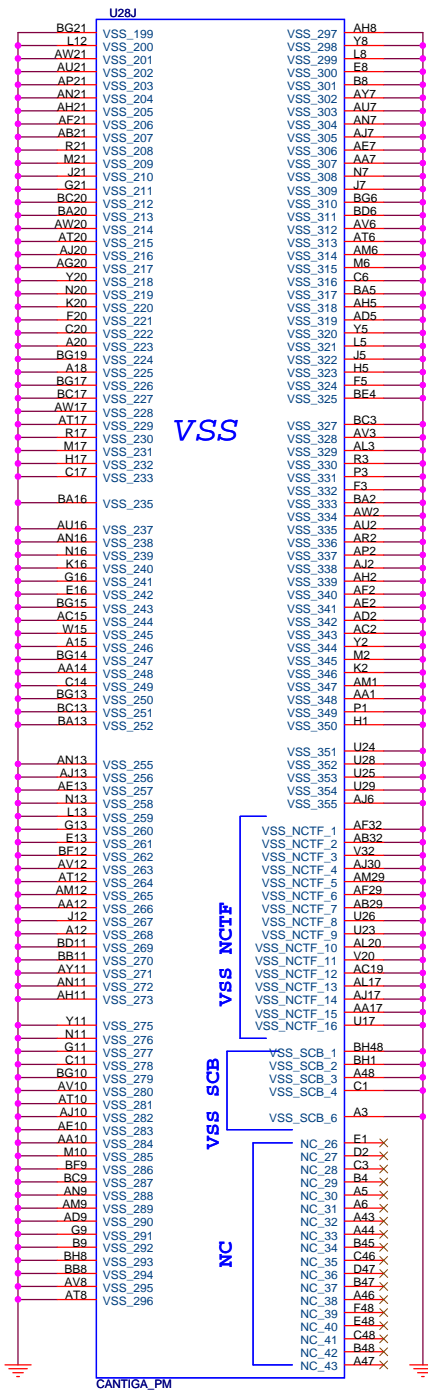
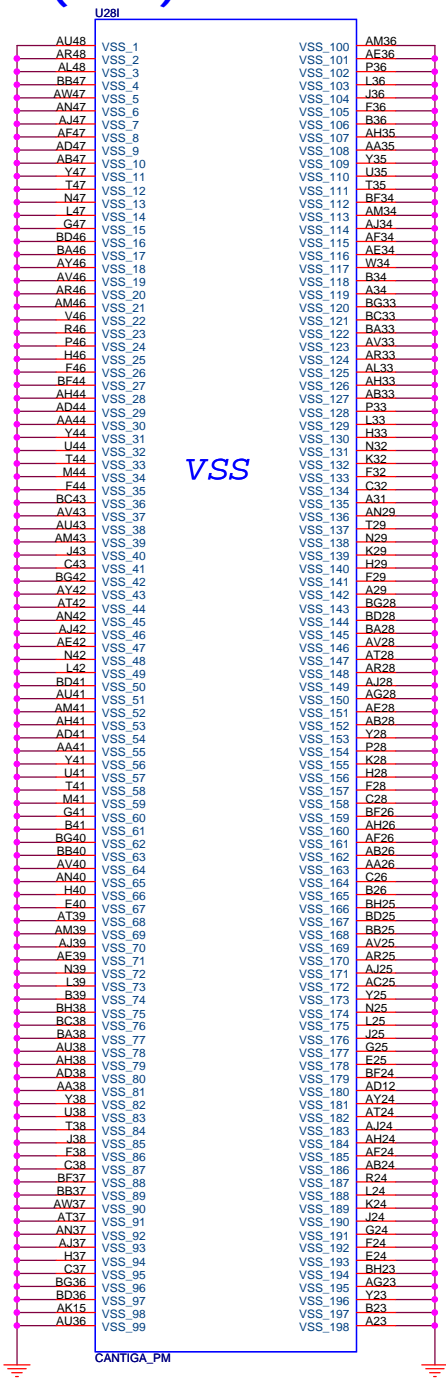
		Quanta Computer Inc. PROJECT : ZR6	
Size	Document Number	GMCH VCC,NCTF	
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		Rev 1/	

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VCCSYNC_CRT	GND
VCCA_CRT_DAC	GND
VCCD_LVDS	GND
VCC_TX_LVDS	GND
VCCA_LVDS	GND
VCCA_TVDAC	GND
VCCD_QDAC	GND
VCCA_DAC_BG	GND
VCC_AXG	GND
VCC_AXG_NCTF	GND

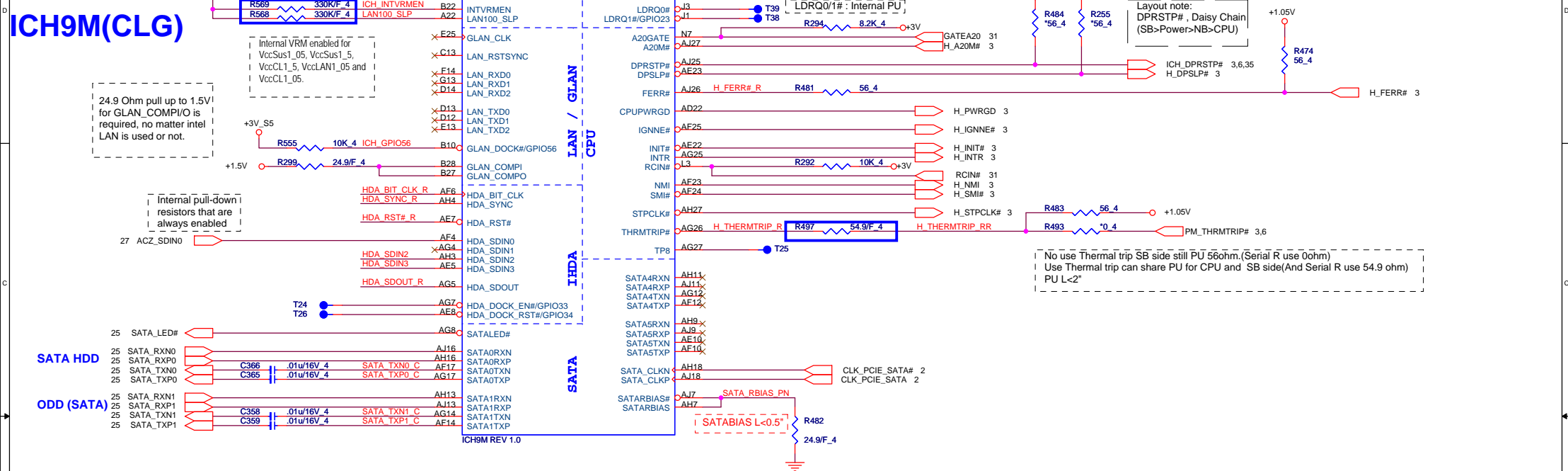


GMCH-CANTIGA(CLG)

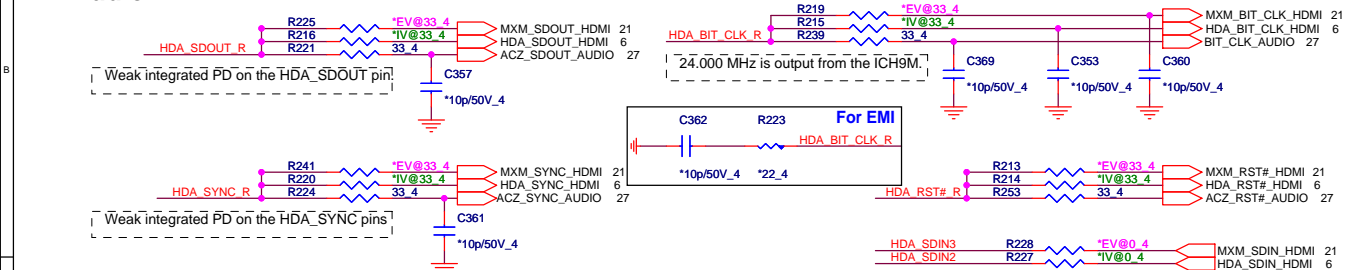


IV@
EV@

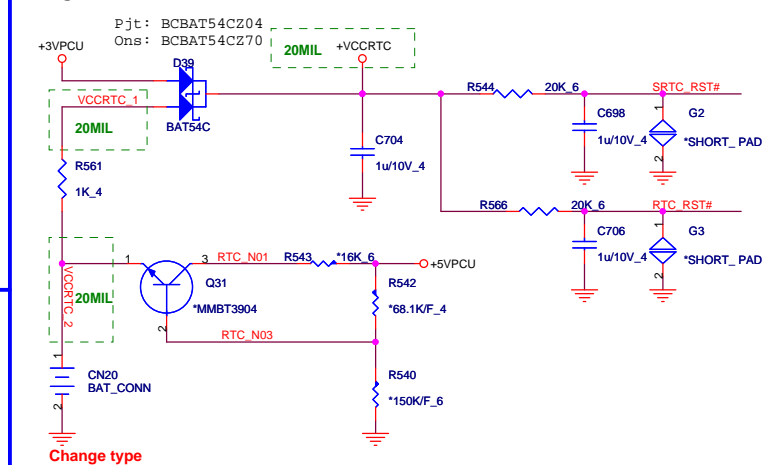
ICH9M(CLG)



HD Audio

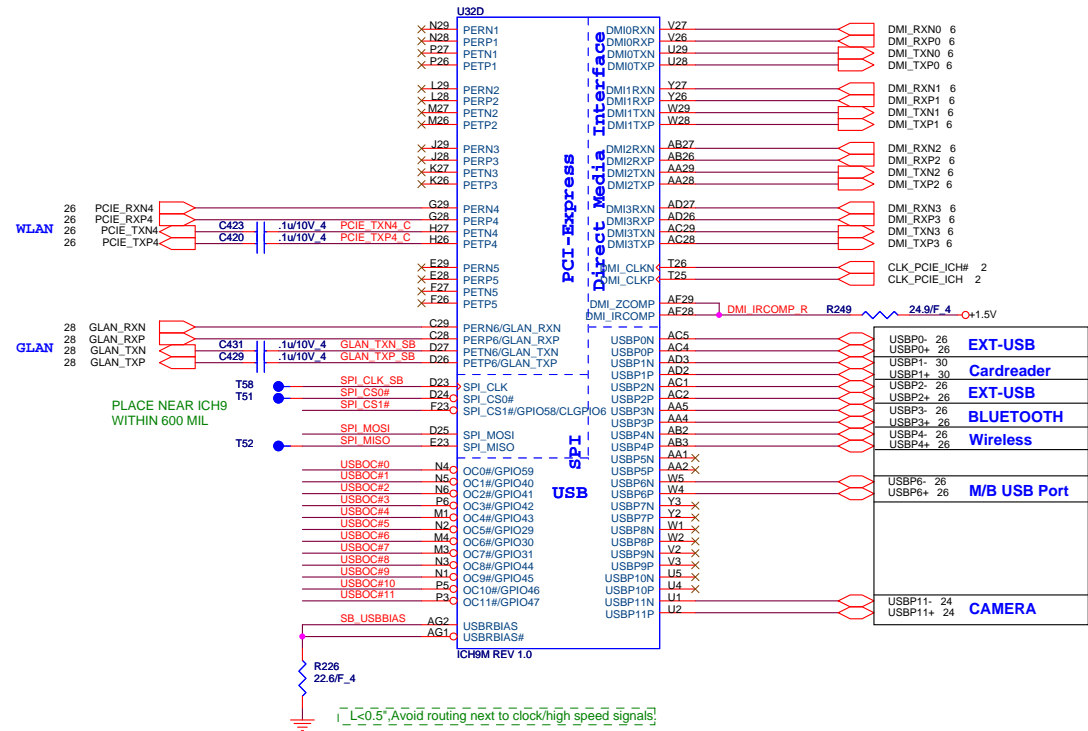


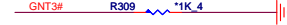

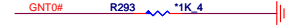

RTC



South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
TP3	XOR Chain Entrance	PWROK	ICH_TP3	ICH_TP3
HDA_SDOUR	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK	HDA_SDOUR	HDA_SDOUR

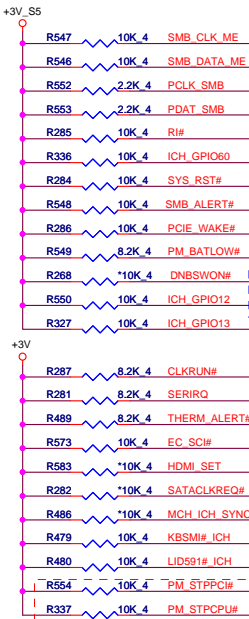


Pin Name	Strap description	Sampled	Configuration			PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0			
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default			
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default			
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default			
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable			
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0	SPI_CS#1	Boot Location	
			0	1	SPI	
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	1	0	PCI	
			1	1	LPC(Default)	

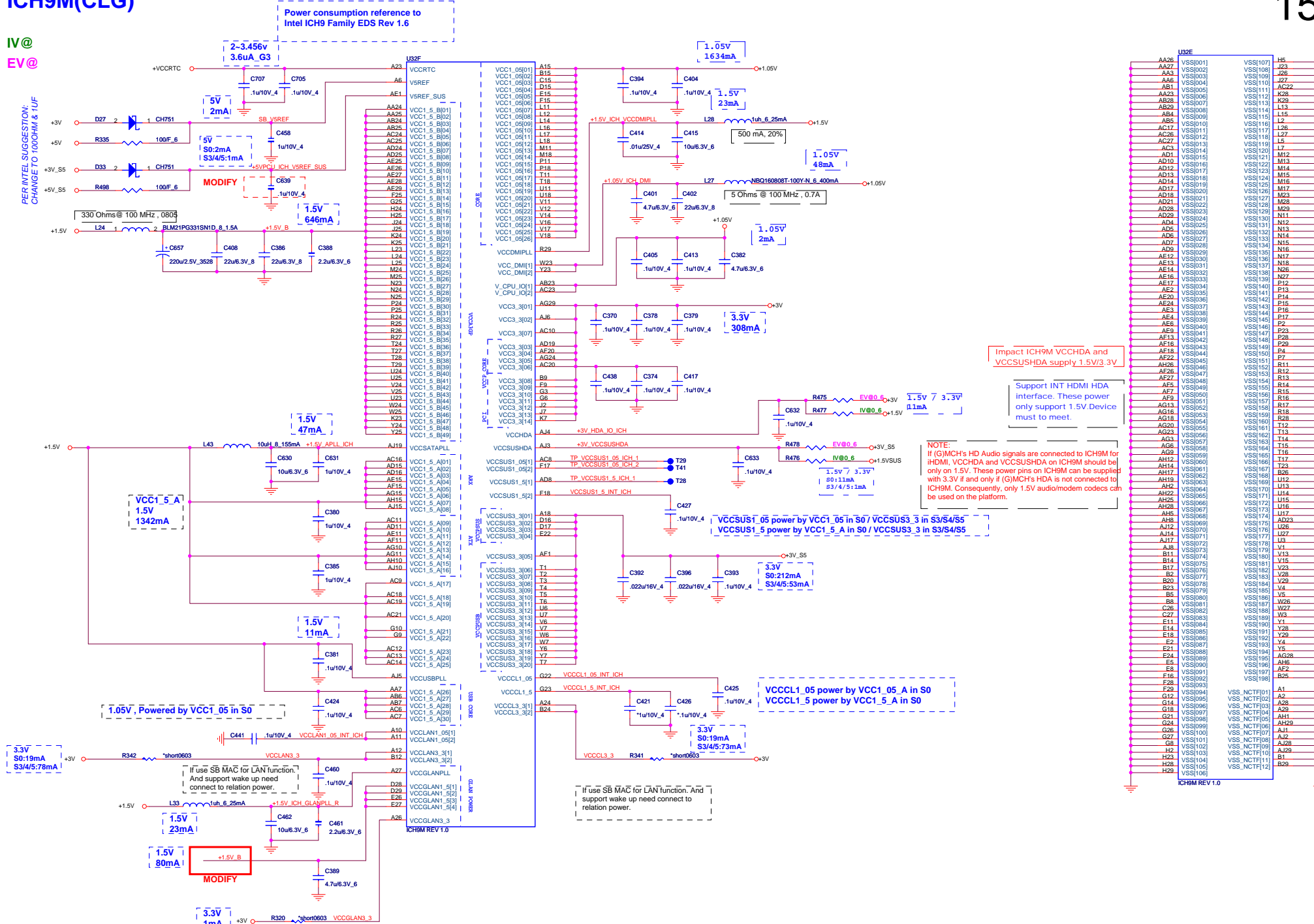
ICH9M(CLG)

D3A:(1/31) ASF issue:when IAMT is not implemented,
ICH9M SMBus and SMLink should be connected together to support slave mode
Connect SMLINK0 to SMBCLK and SMLINK1 to SMBDATA (Add R474,R475 for debug use)

SATA[x]GP pins if unused may be
8.2k to 10k pull-up to Vcc3.3 or
8.2k to 10k pull-down to ground

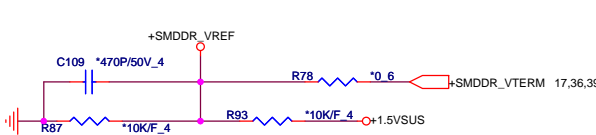
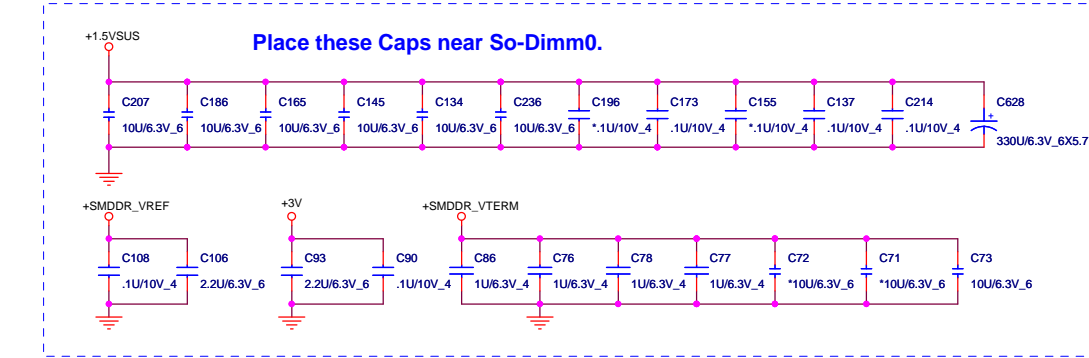
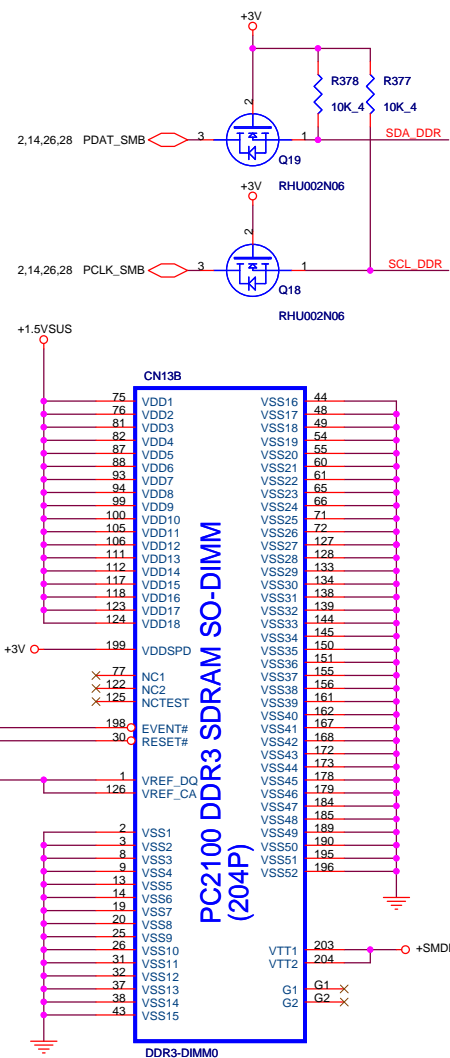
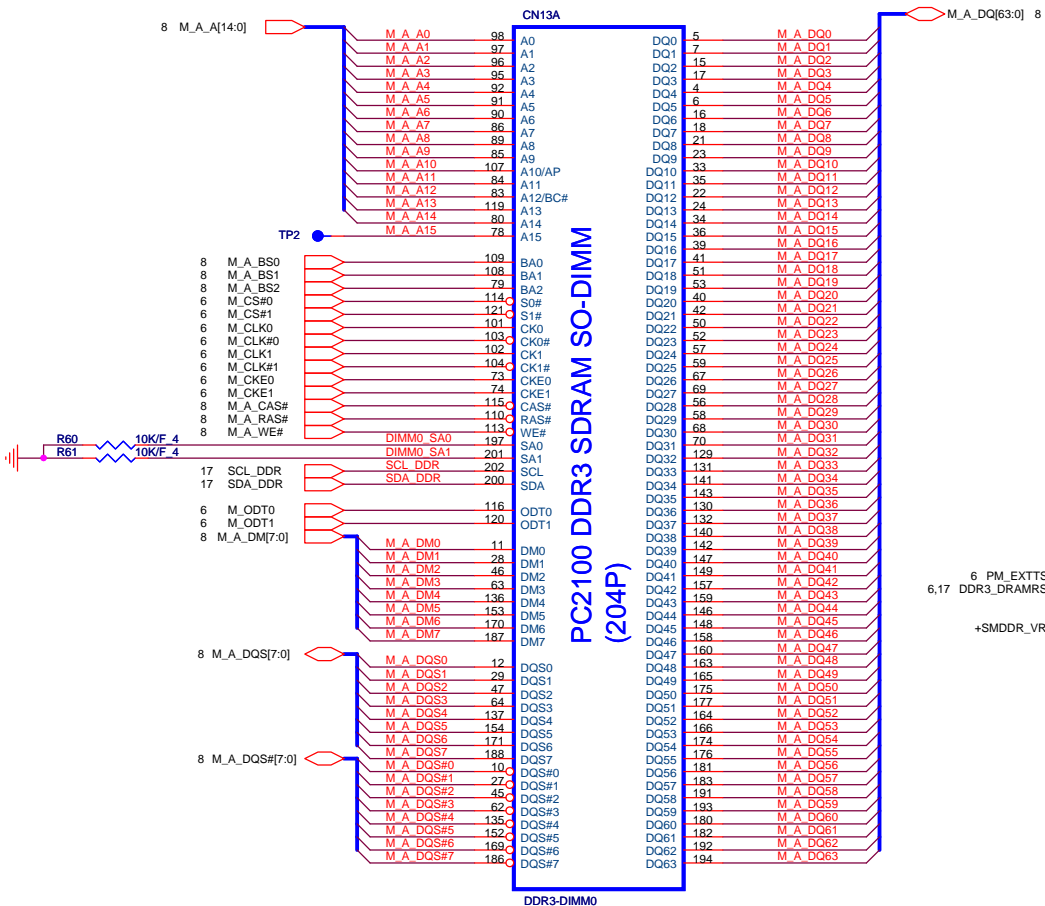


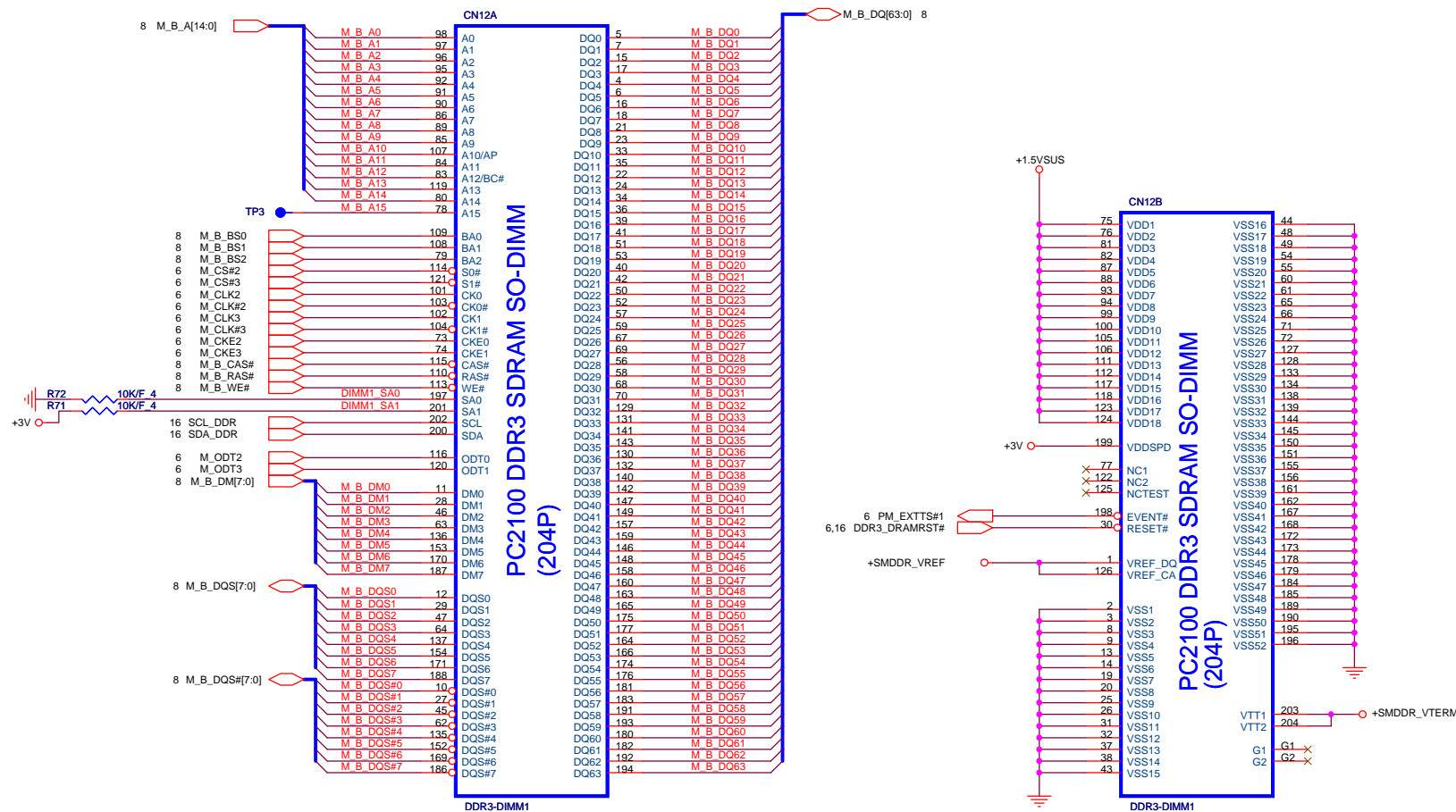
EV@

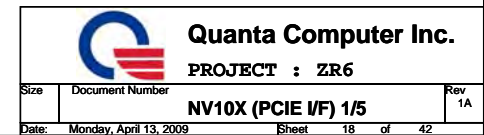


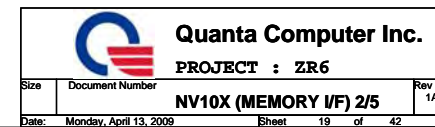
DDR3 (DDR)

16

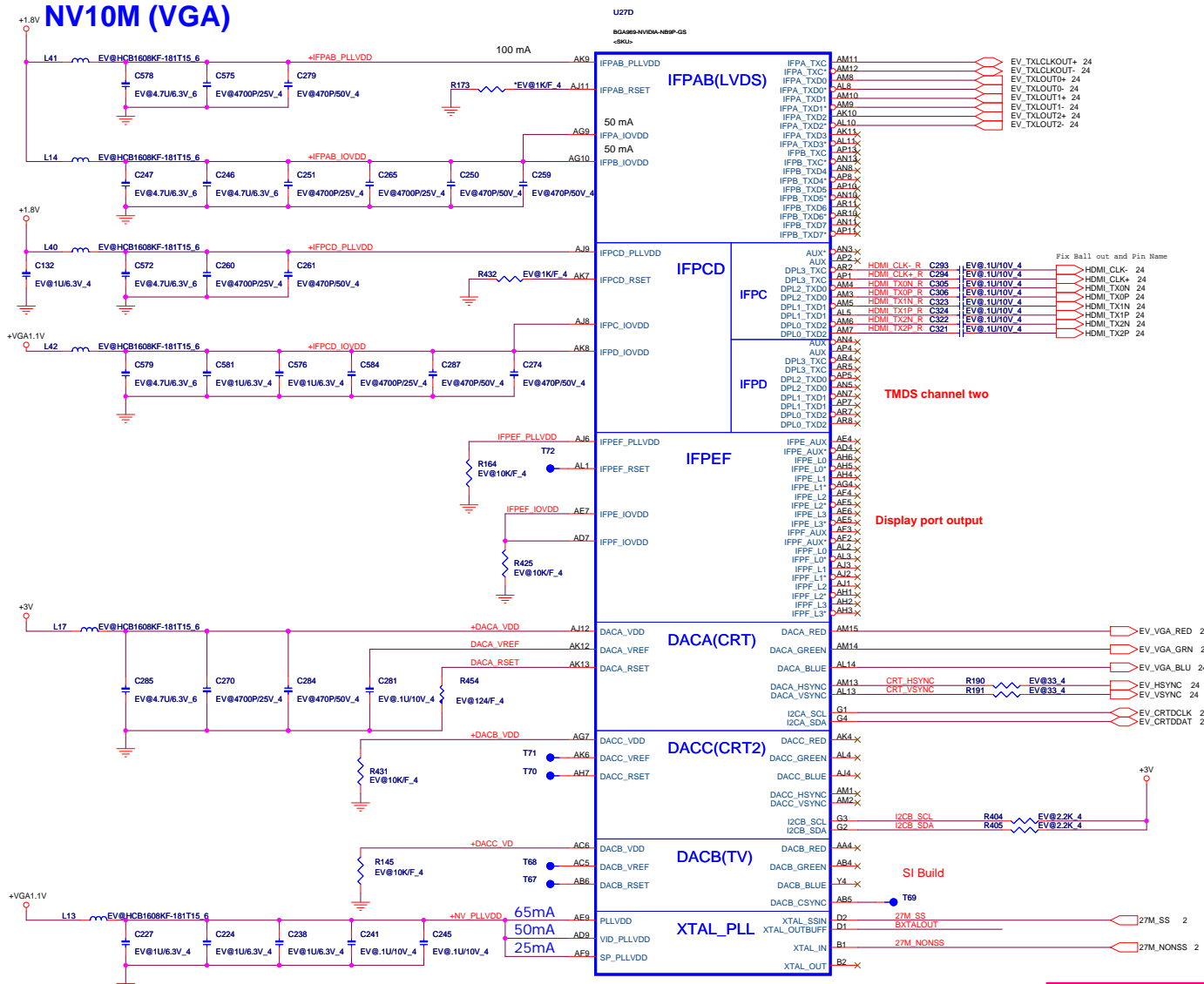








NV10M (VGA)

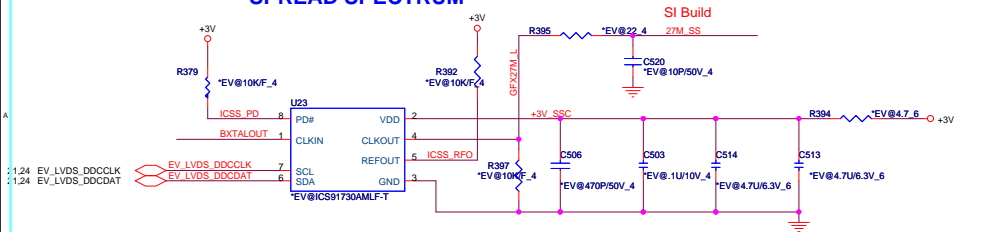


TMD5 channel two

Display port output

SI Build

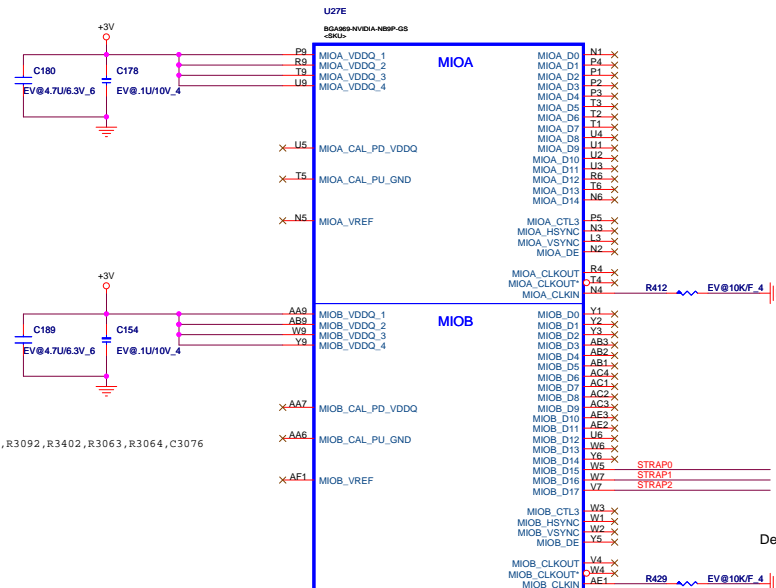
SPREAD SPECTRUM



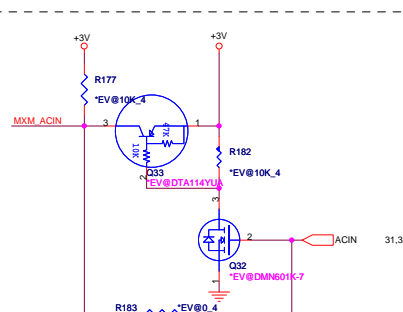
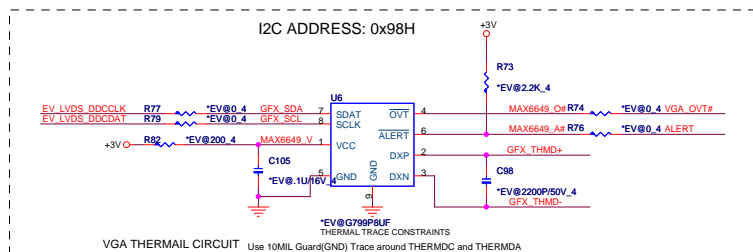
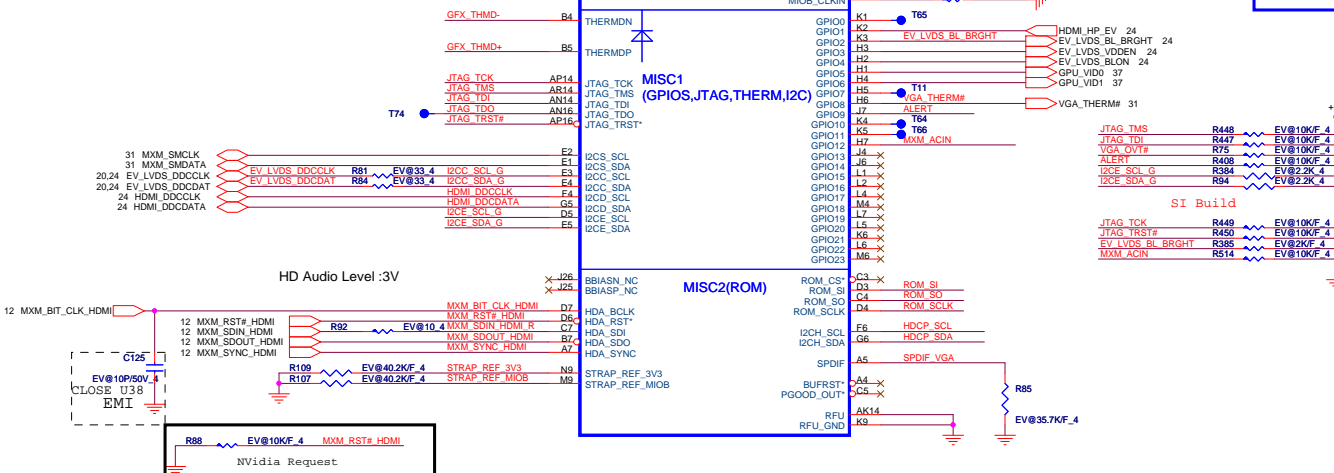
I2C ADDRESS: 0xD4H

Nvidia suggest:
10 kΩ pull-down only if
no spread chip used.

The diagram shows two signal lines, 27M_SS and BXTALOUT, each with a pull-down resistor connected to ground. The resistor for BXTALOUT is labeled R391 EV@10K.F.4. The resistor for 27M_SS is labeled R396 EV@10K.F.4.

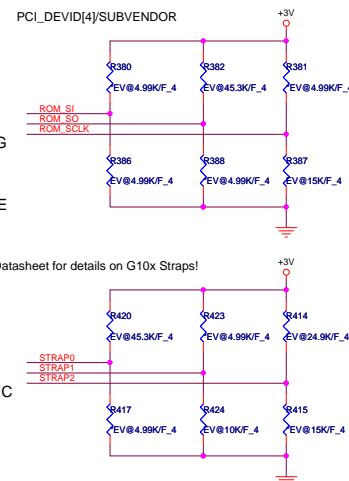


NVidia Propose Remove C3134.C3681.R3092.R3402.R3063.R3064.C3076



N10P-GE1 (G96) Straps

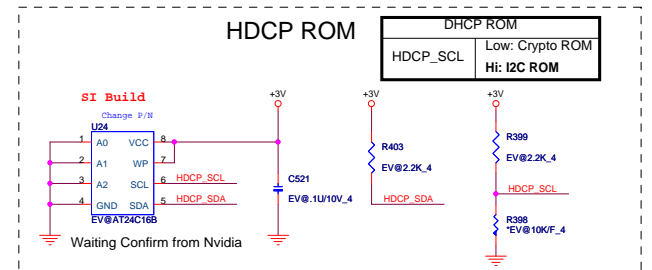
GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL



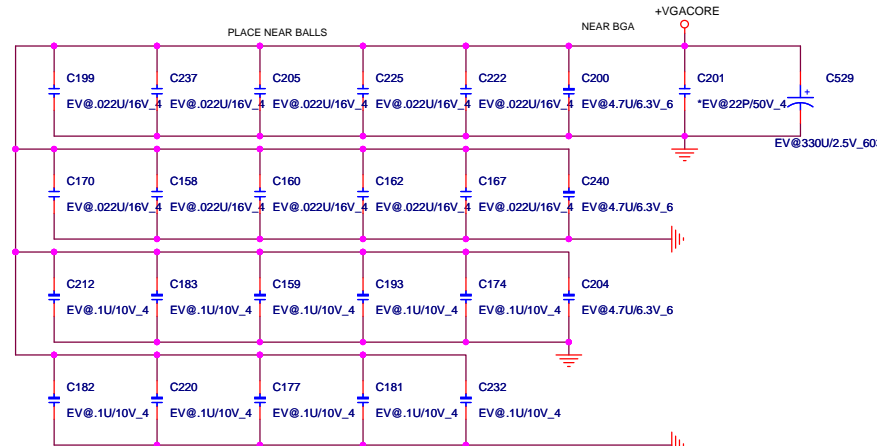
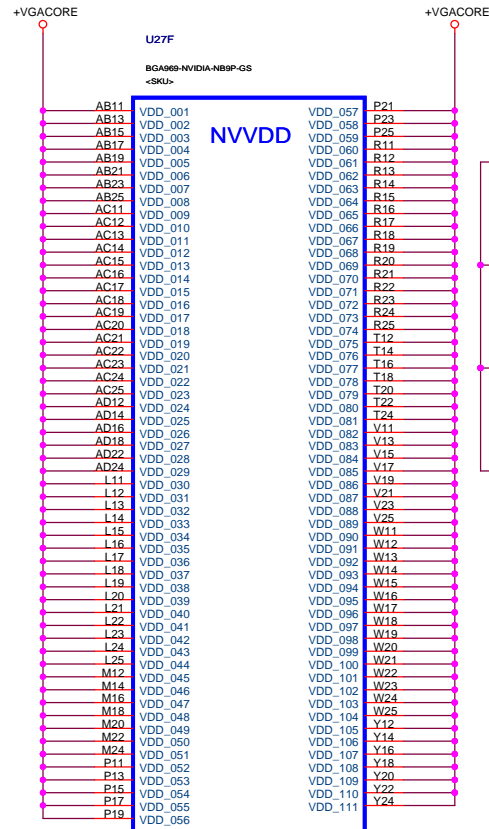
SEE Datasheet for details on G10x Straps!

			Logical Strap Bit Mapping		
			R414	PU-VDD	PD
PCI_DEVID:	STRAP2				
NB9M-GE	0x06E 8	1000	5K	1000	0000
NB9M-GS	0x06E 9	1001	10K	1001	0001
NB9P-GE2	0x064 8	1000	15K	1010	0010
NB9P-GE2	0x064 8	1000	20K	1011	0011
NB9P-GS	0x064 9	1001	25K	1100	0100
N10P-GE1	0x065 2	0010	30K	1101	0101
N10M-GE1	0x06E C	1100 default	35K	1110	0110
			45K	1111	0111

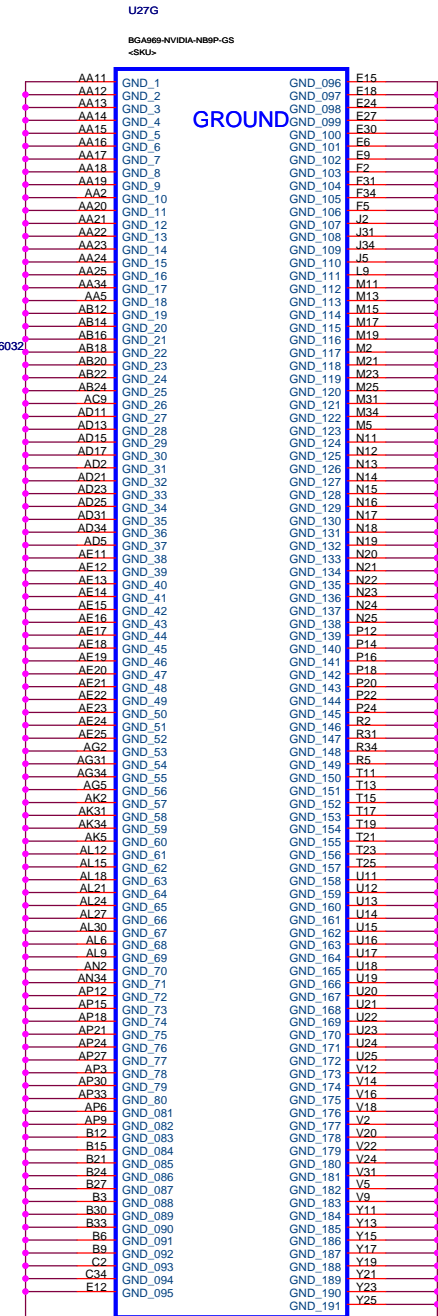
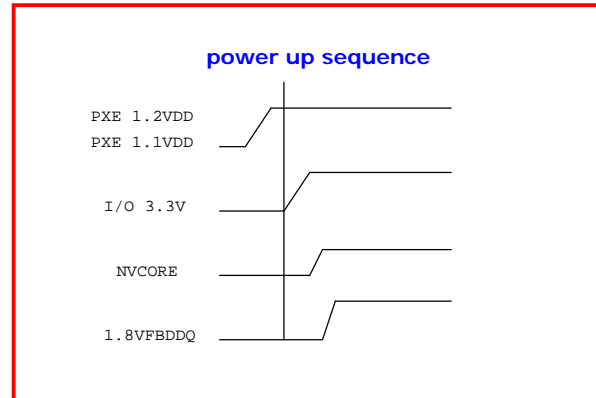
R386	Config	Definitions	Die
CS25102FB02 5K	64Mx16 DDR2	Hynix	E
CS31002FB26 10K	64Mx16 DDR2	Samsung	Q
CS32002FB29 20K	64Mx16 DDR2	Samsung	E



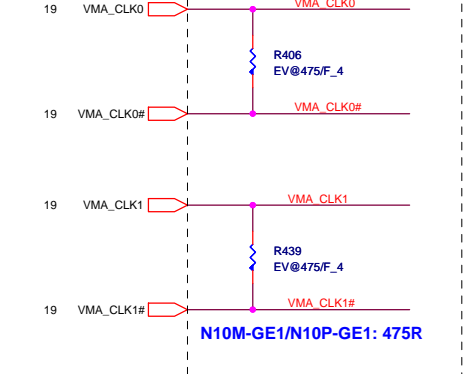
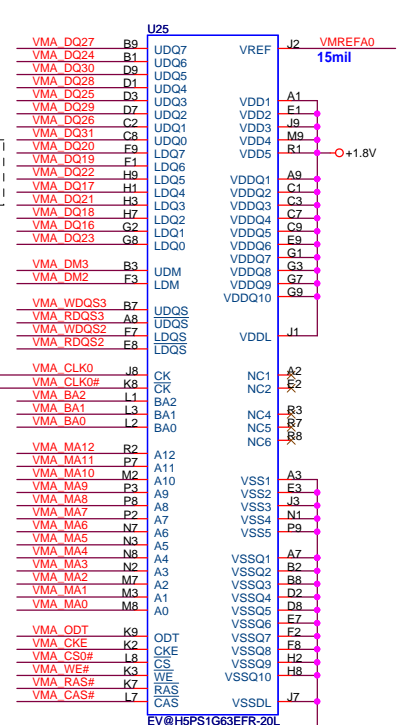
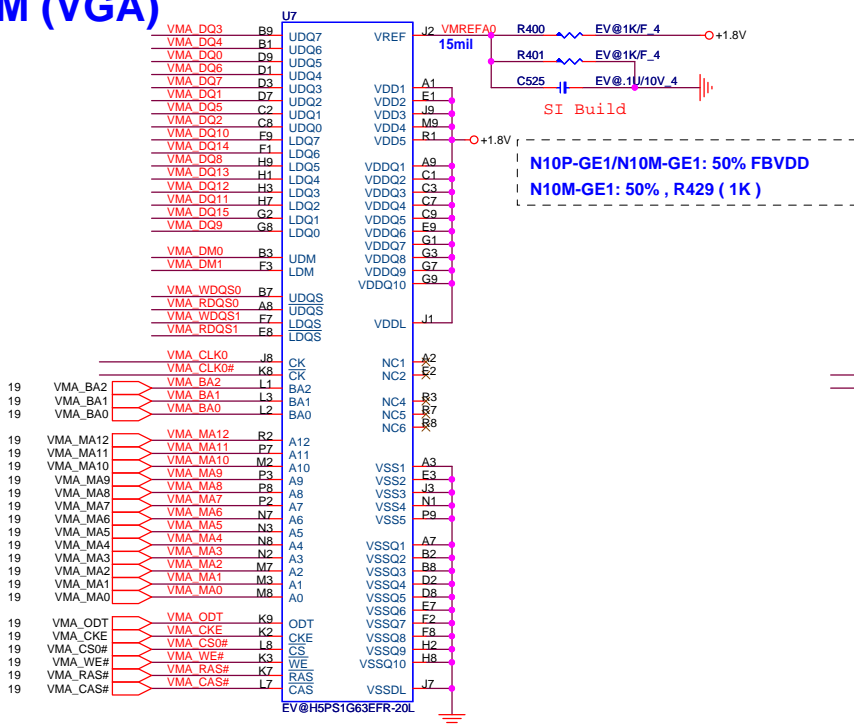
NVVDD Decoupling



Follow Design Guide DG-03276-001 4.7uFx3 and 0.22x10 uF instead of 0.1uF x10

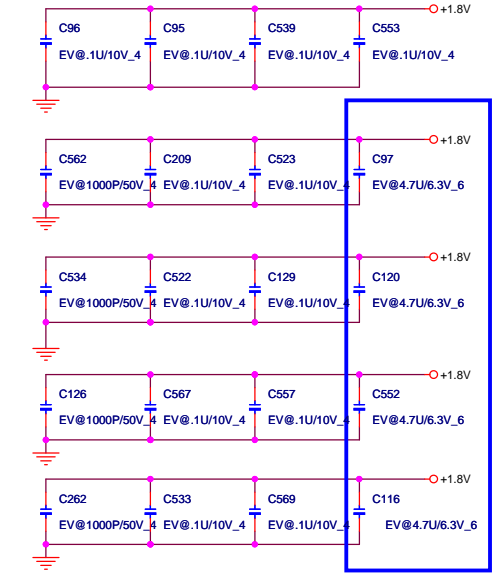


NV10M (VGA)

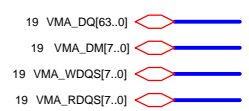
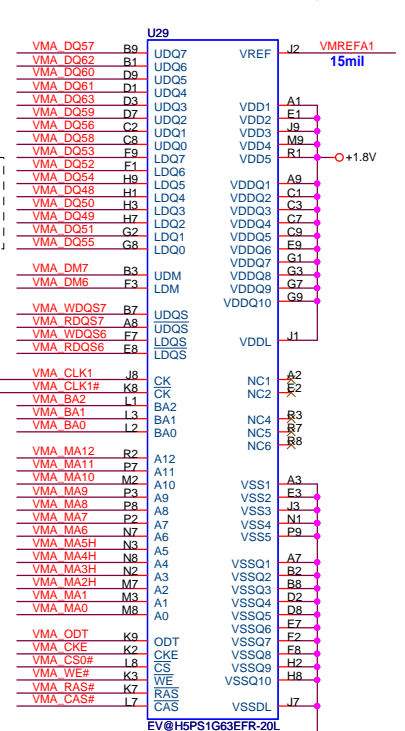
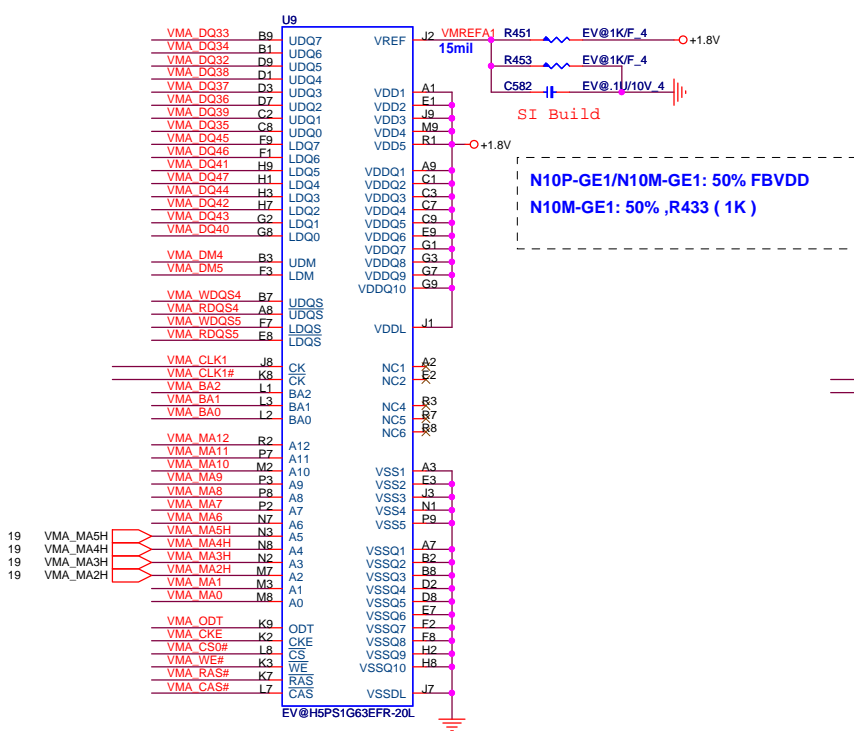


CS14752FB11 RES CHIP 475 1/16W +1% (0402)

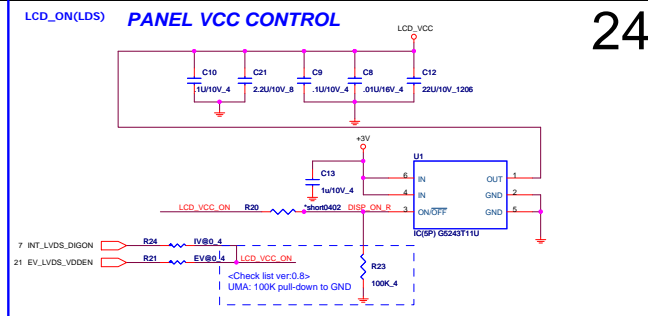
(By pass capacitor)



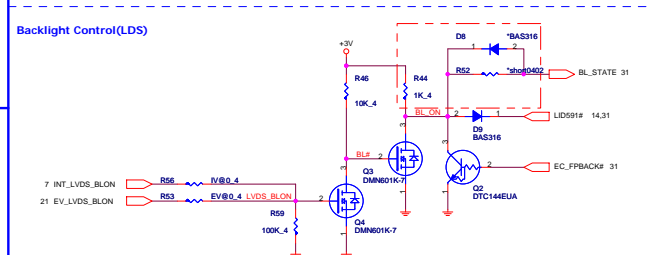
For DB:
 N10P/N10M : AKD5LG-T510(Samsung,64M*16)
 AKD5LG-TW02(Hynix,64M*16)



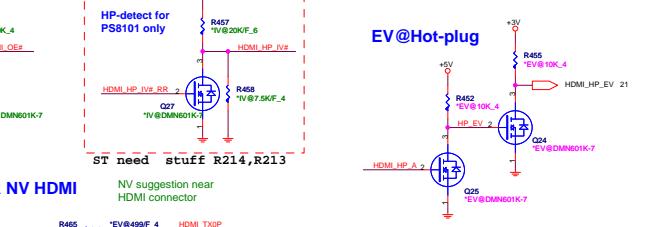
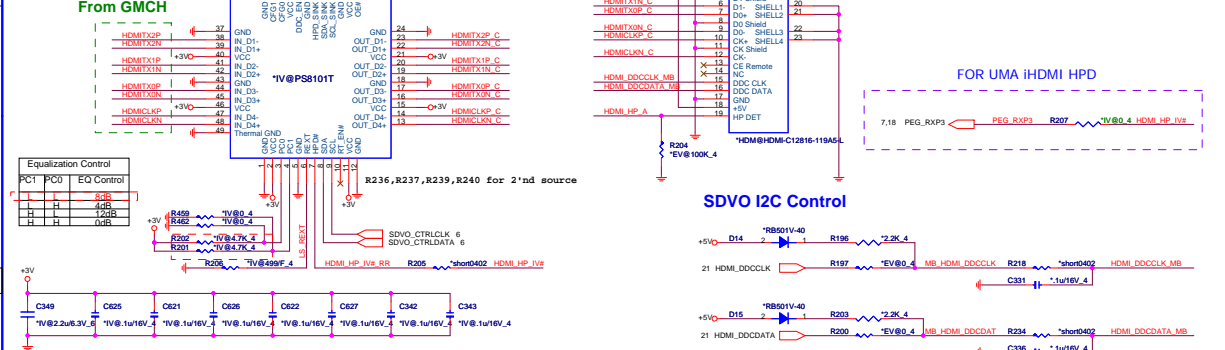
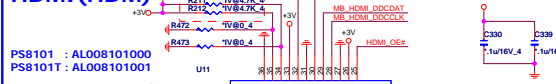
24



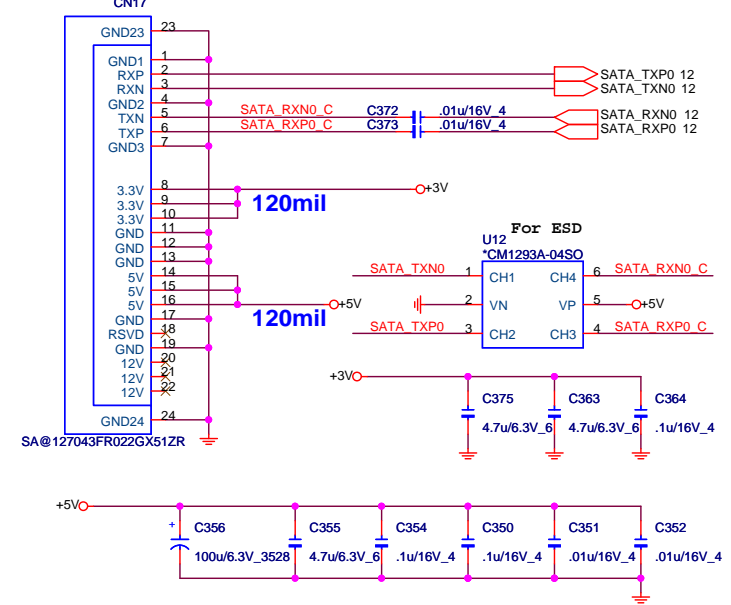
Backlight Control(LDS)



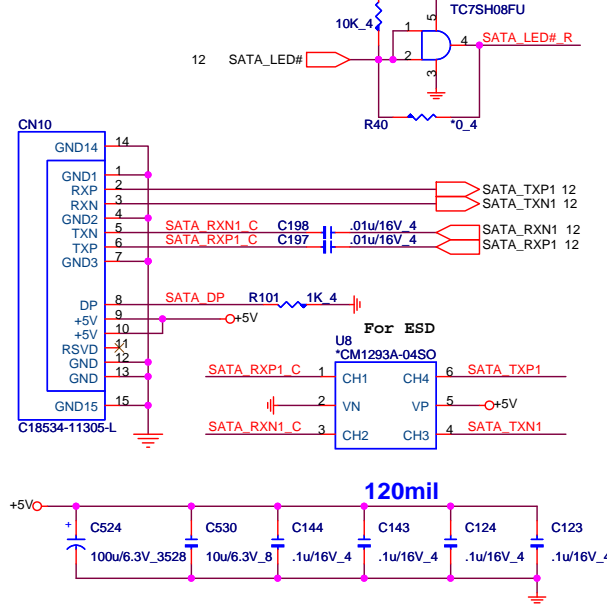
HDMI (HDM)



SATA HDD(HDD)

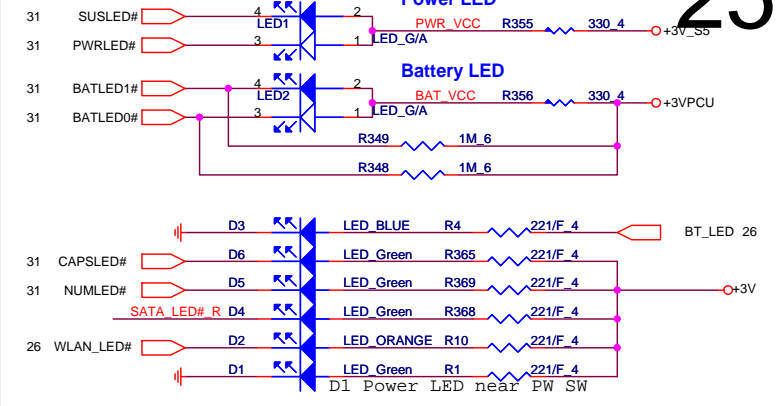


SATA ODD(ODD)

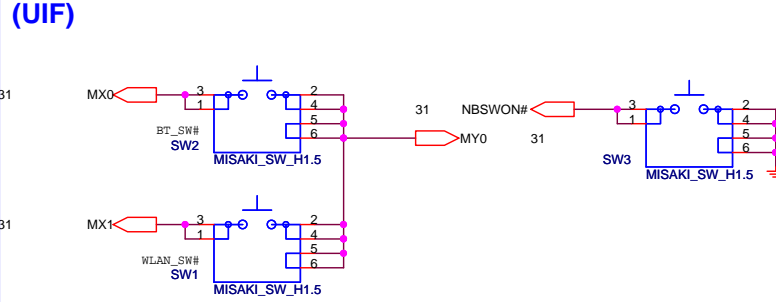


LED(UIF)

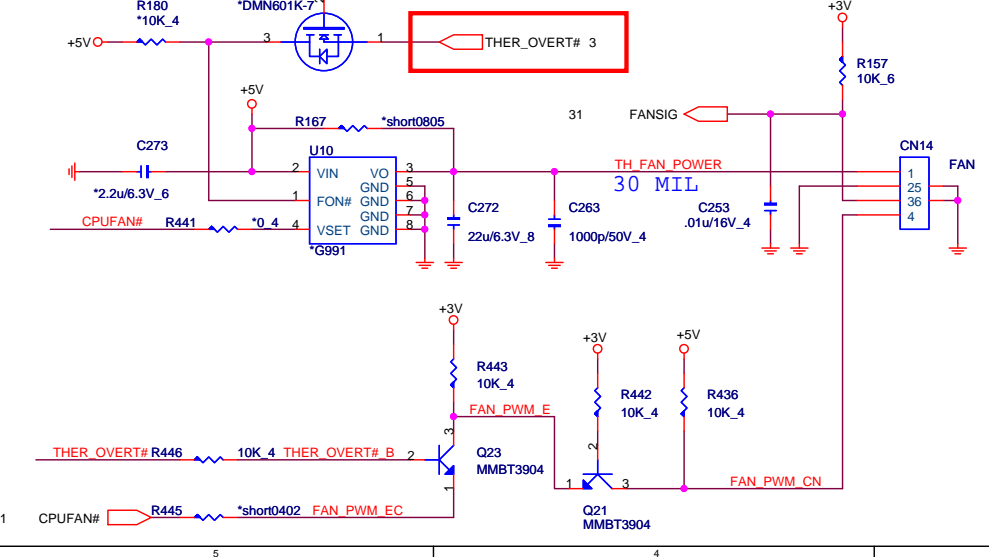
Power / Suspend : Green / Amber



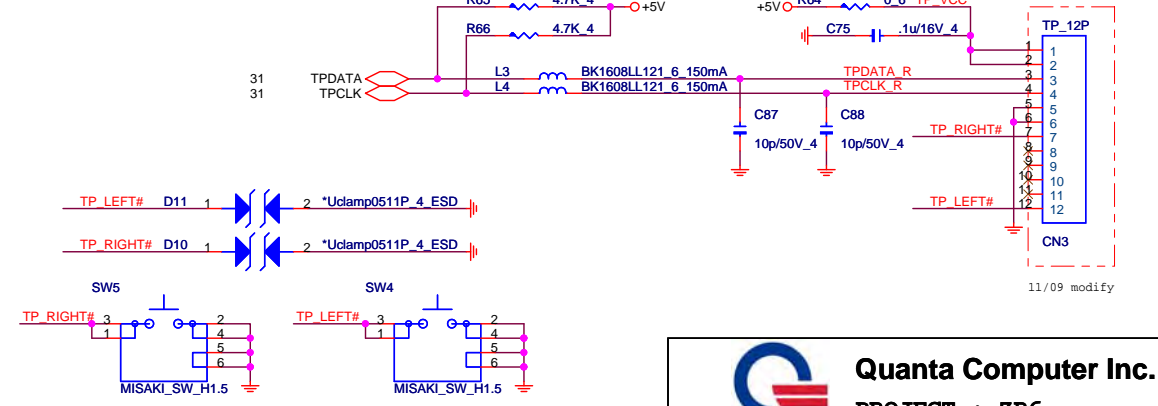
Power Button (UIF)



FAN(THM)



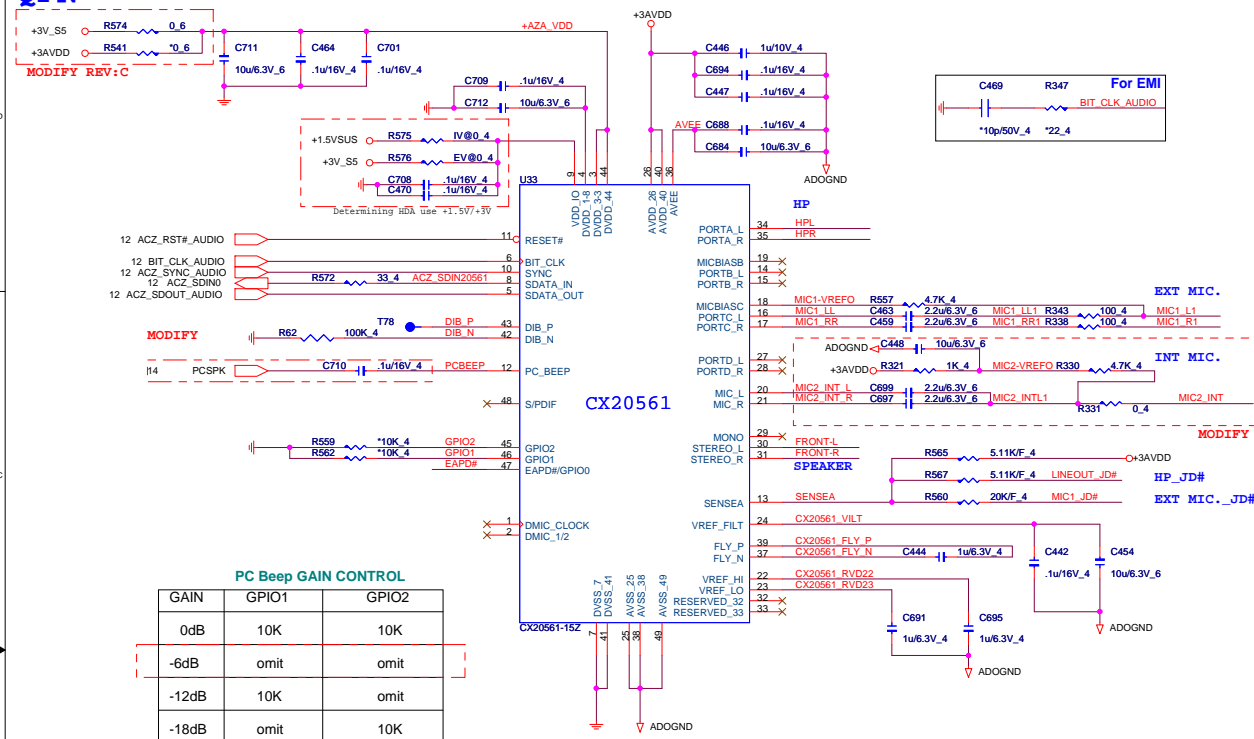
TP CONN



Quanta Computer Inc.
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	HDD/ODD/LED/SW/TP/FAN/MMB	1A
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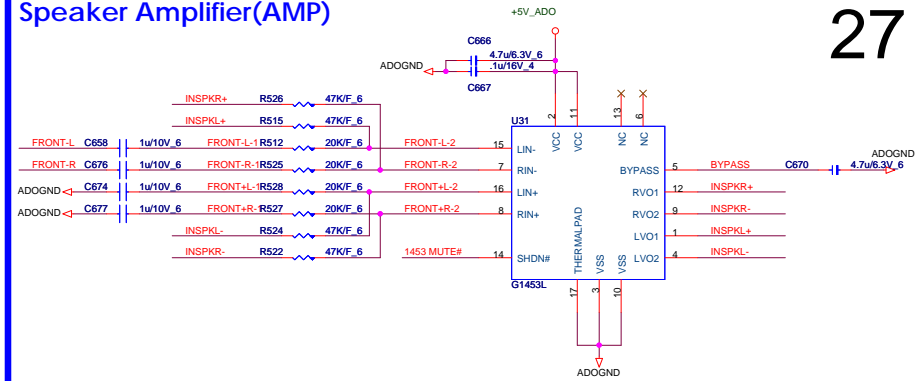
QFN



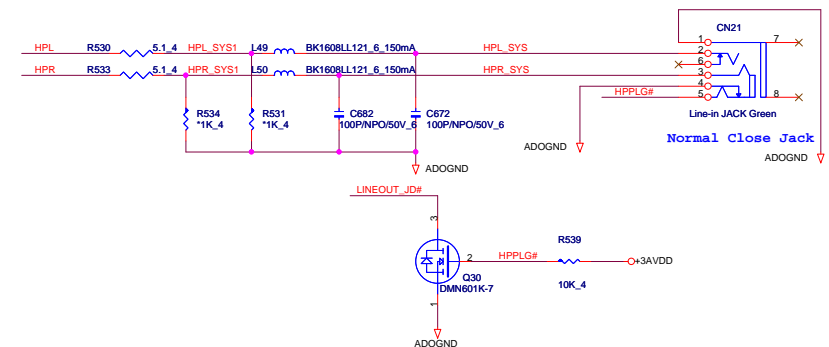
PC Beep GAIN CONTROL

GAIN	GPIO1	GPIO2
0dB	10K	10K
-6dB	omit	omit
-12dB	10K	omit
-18dB	omit	10K

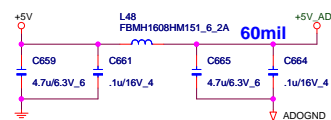
Speaker Amplifier(AMP)



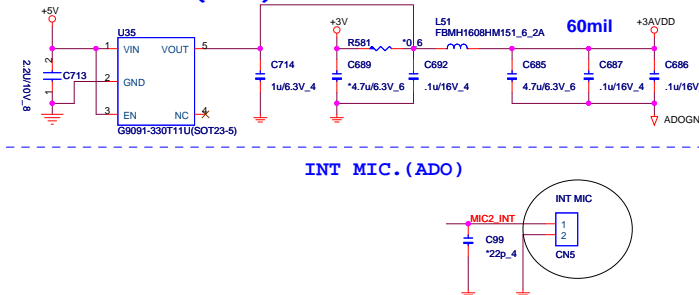
LINE OUT(AMP)



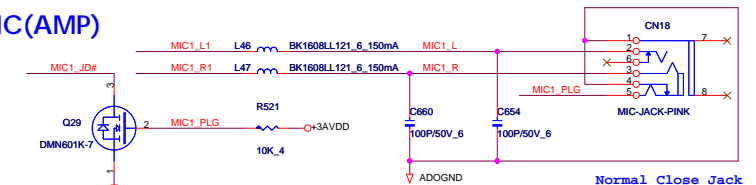
AMP Power(AMP)



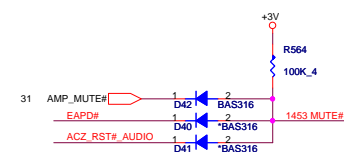
CODER Power(ADO)



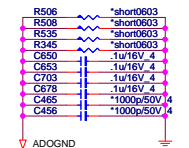
MIC(AMP)



MUTE (AMP)



(ADO)



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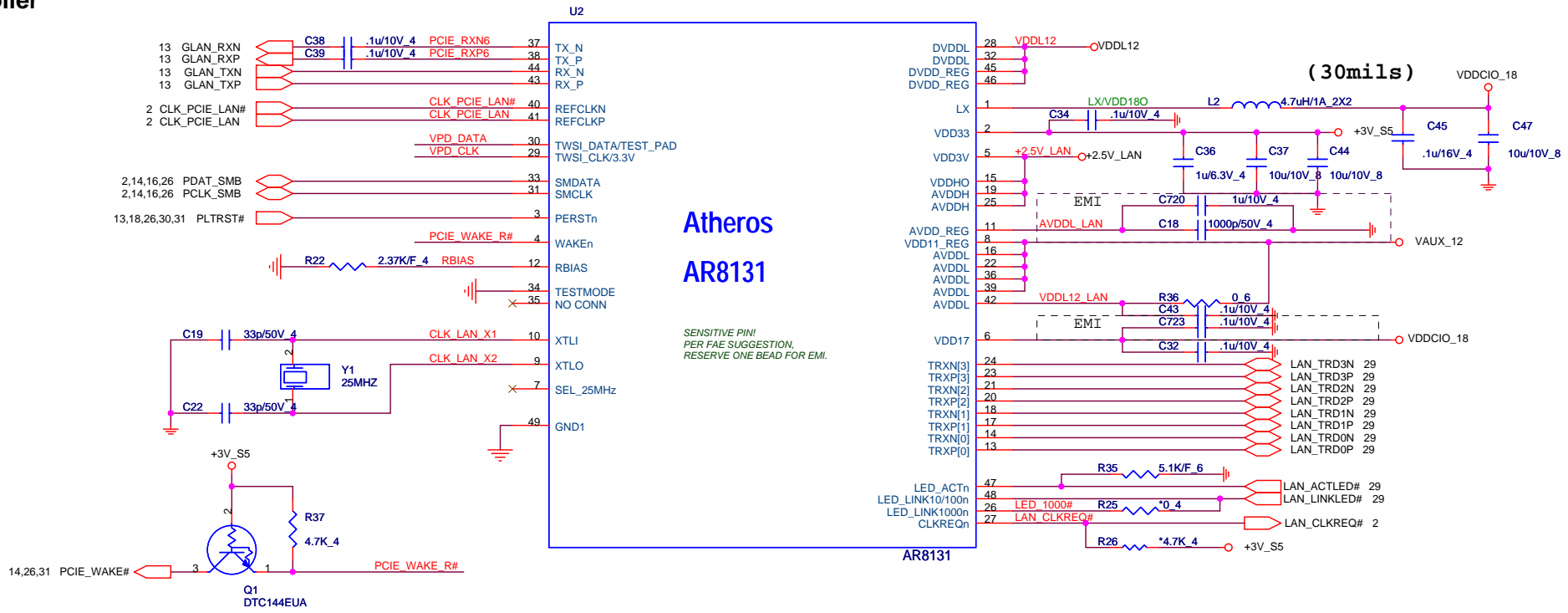
PROJECT : ZR6

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	CODEC/AMP/MDC	1A
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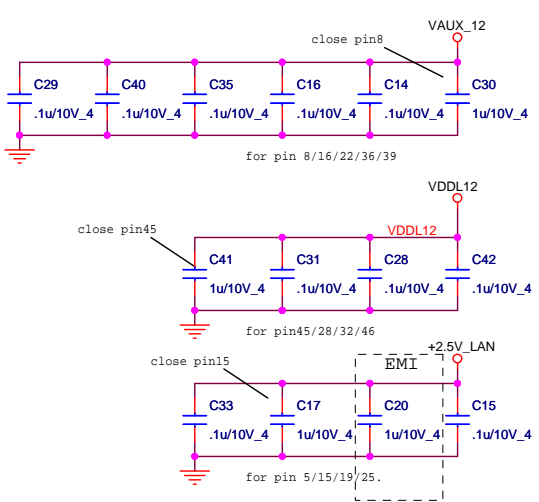
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1

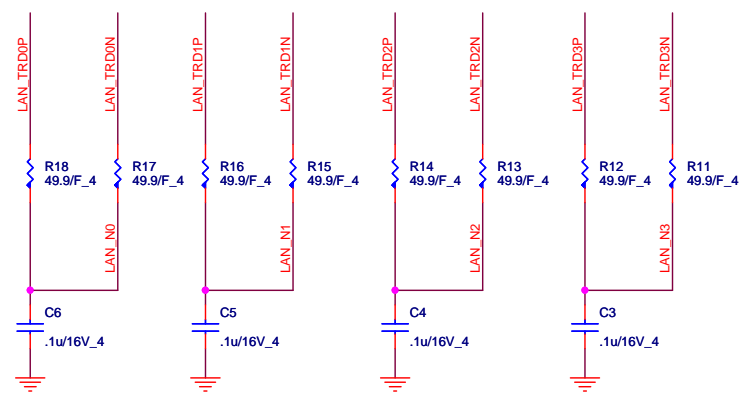
LAN Controller



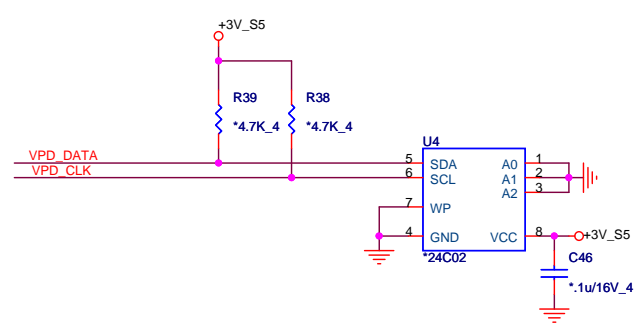
Decoupling CAP



PLACE NEAR IC SIDE



EEPROM



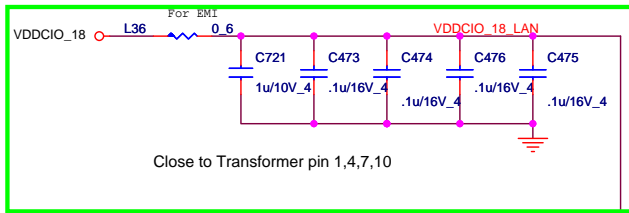
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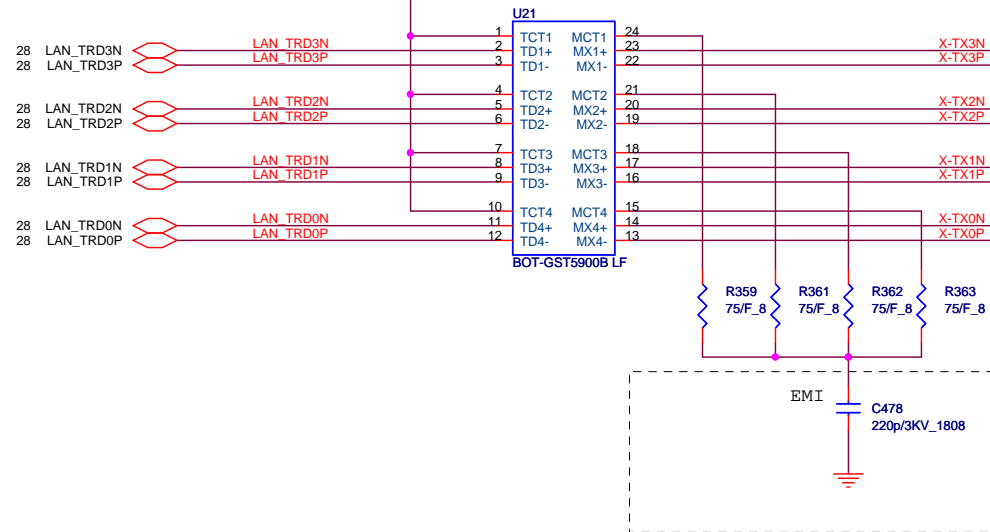
AR8131 GLAN

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		1A

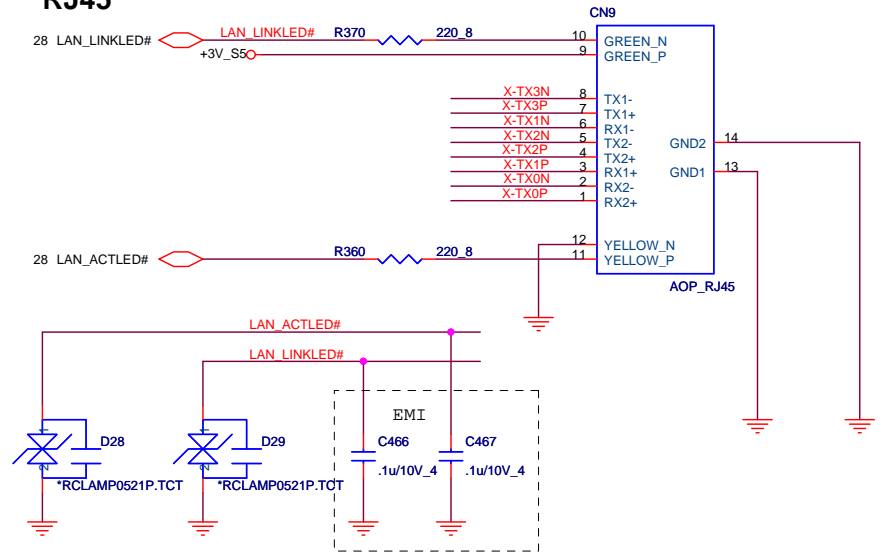
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TRANSFORMER



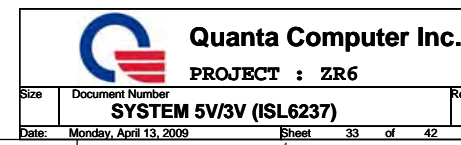
RJ45

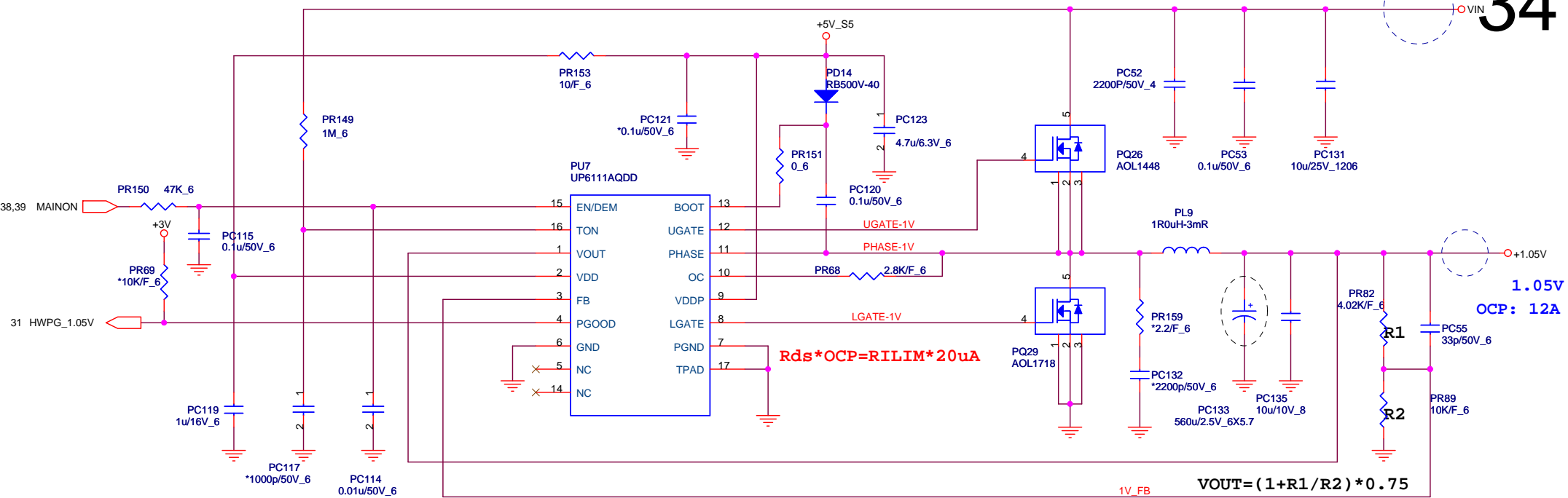


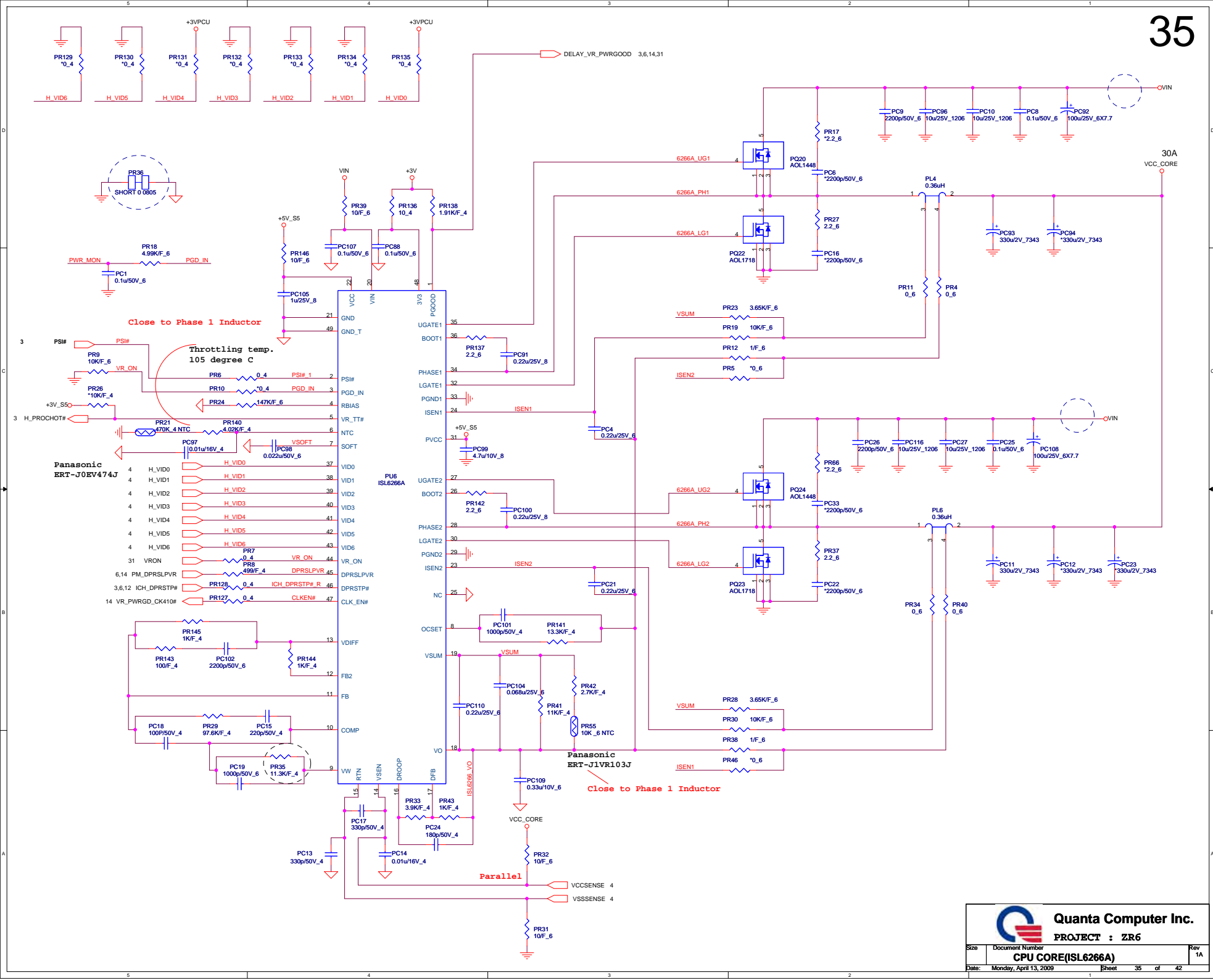
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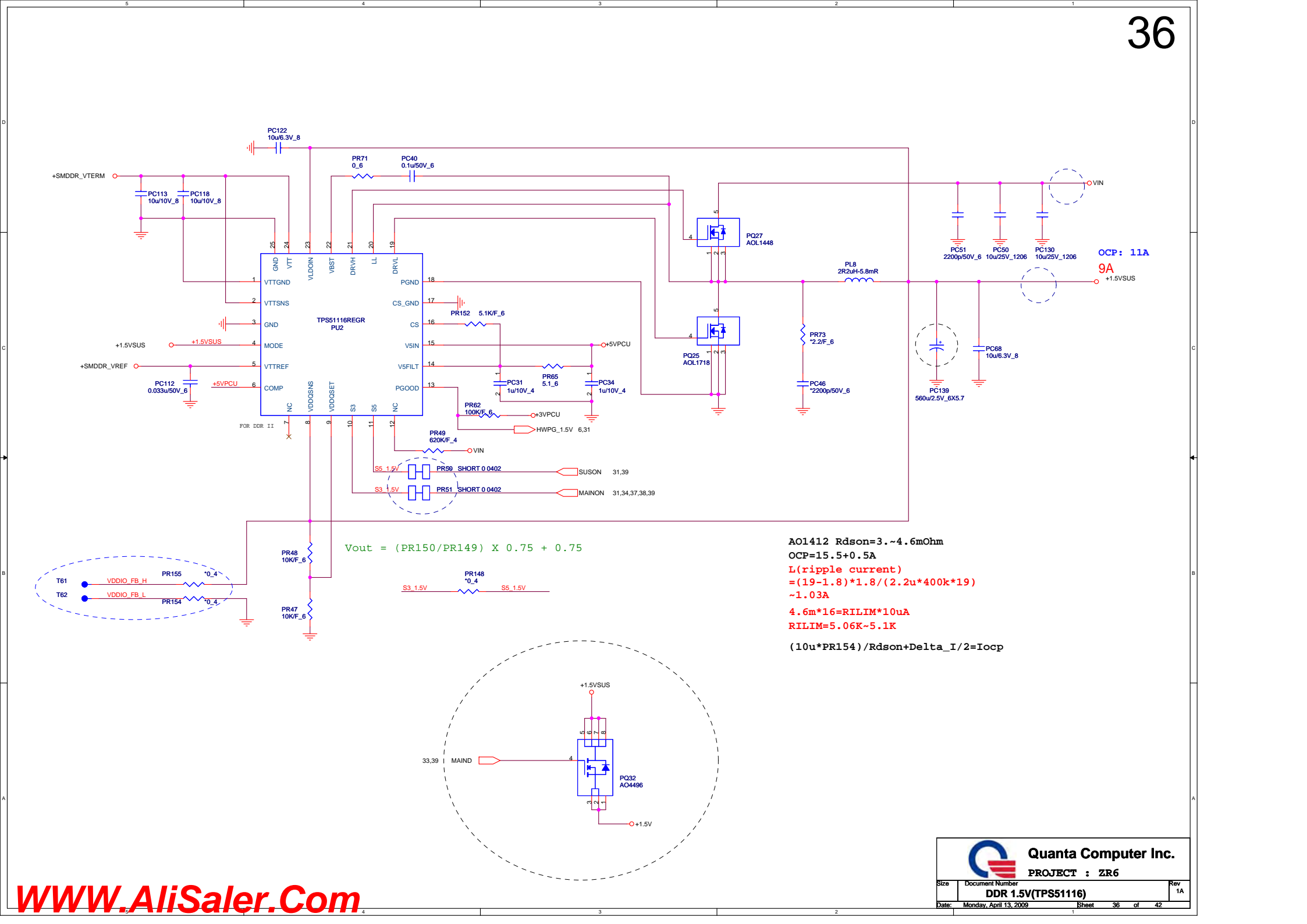
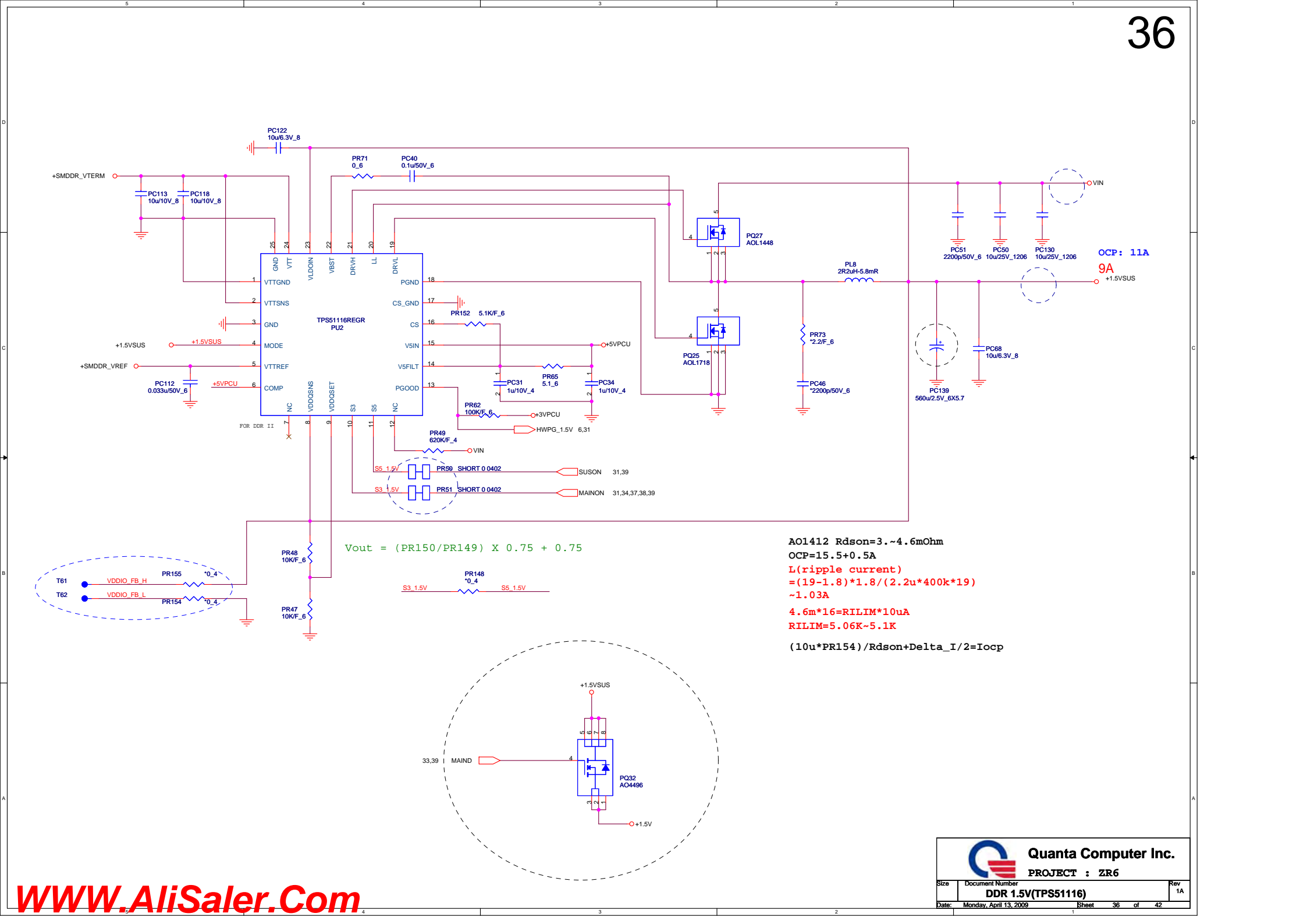
PROJECT : ZR6

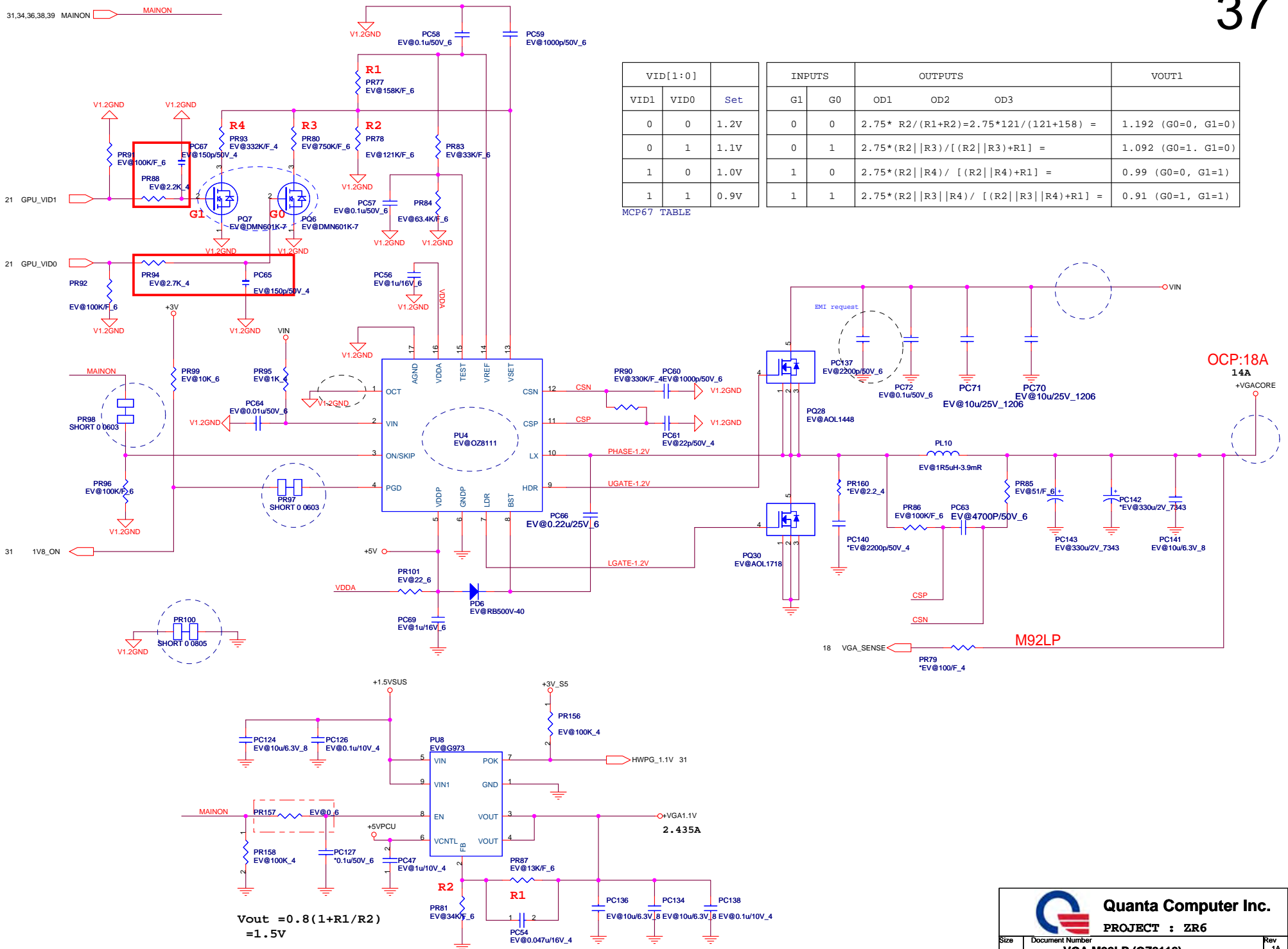
Size	Document Number	Rev
	LAN Transformer and RJ45/BT	1A
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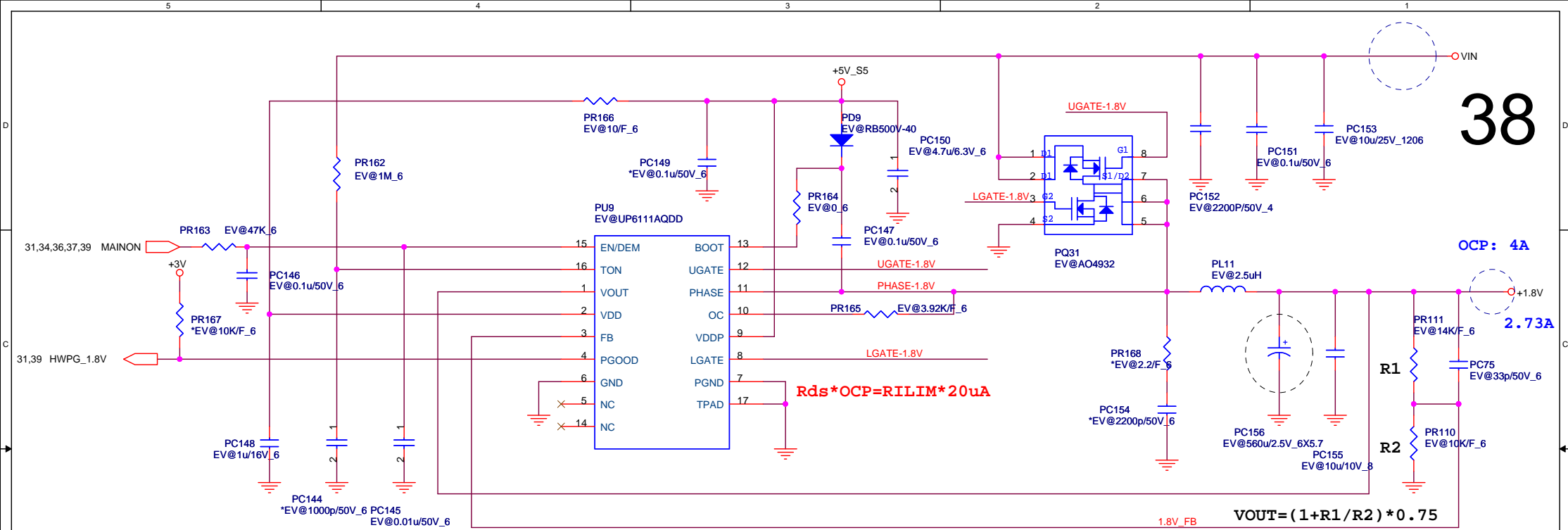












$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin * TON)$$

$$TON = 3.85p * 1M * 1 / (Vin - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$

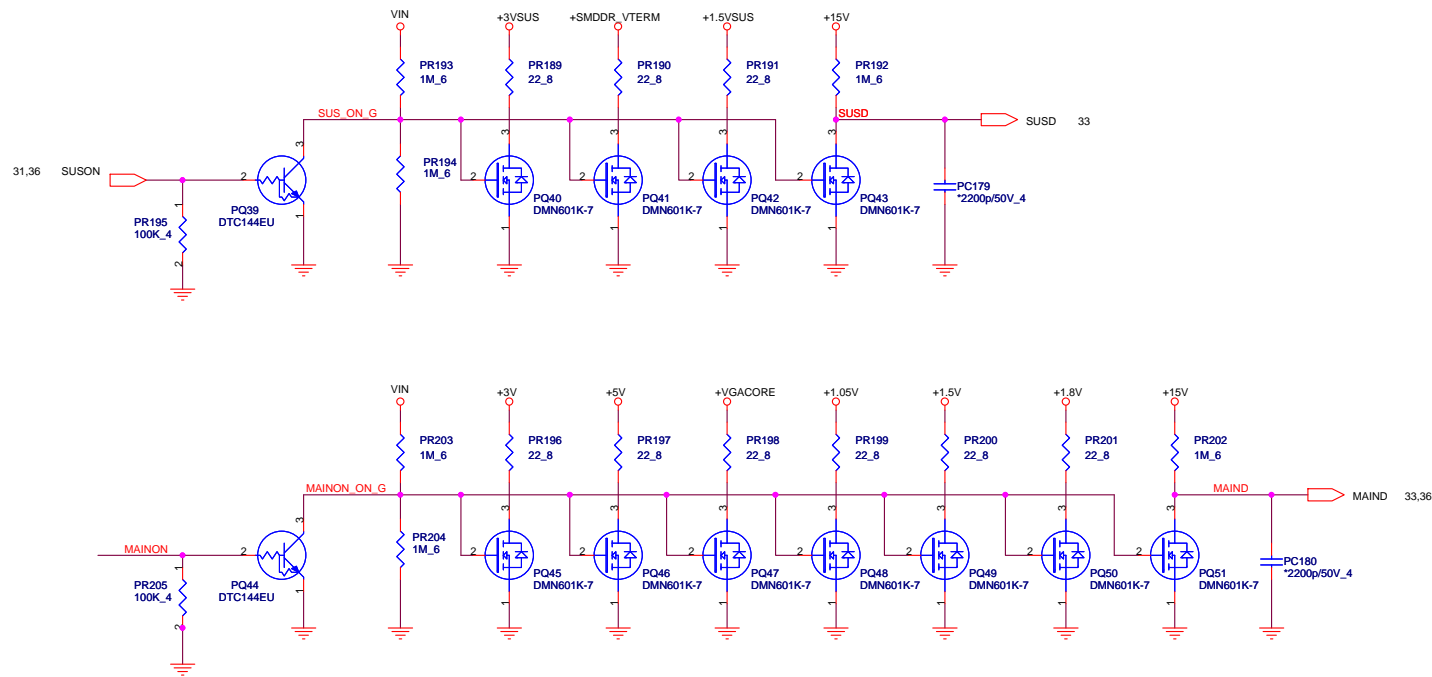
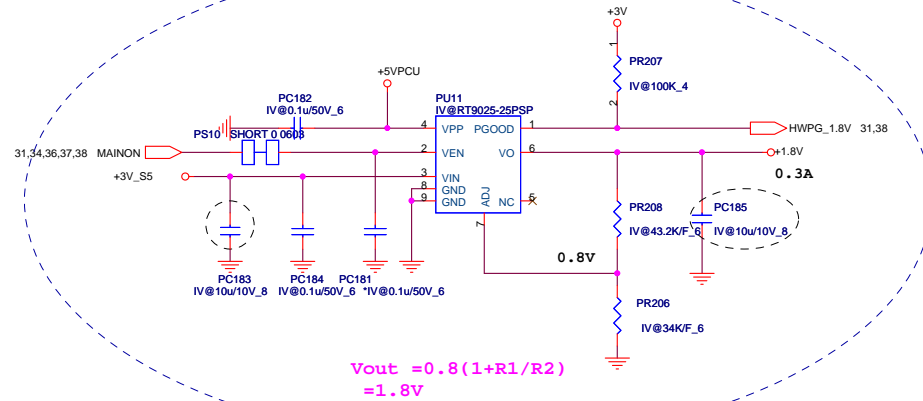
$$AO4932 \text{ } R_{ds} = 15.6 \sim 19.6m\Omega$$

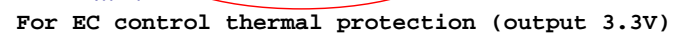
$$OCP = 16 - 0.8A$$

$$L(\text{ripple current}) = (19 - 1.8) * 1.8 / (2.5u * 272k * 19) \sim 2.14A$$

$$19.6m * 4 = RILIM * 20uA$$


$$RILIM = 3.92K$$





MODEL: REV		CHANGE LIST		MODEL	
		PAGE	ZR6 MB		
			FROM	TO	
ZR6 MB	A	1	1A		
		2	1A	3B	
	B	3	1A		
		4	1A		
		5	2A		
		6	1A		
		7	1A		
		8	1A		
		9	3A		
		10	3A		
		11	1A	3B	
		12	1A		
		13	1A		
		14	3A		
		15	2A		
		16	1A		
		17	3A	3B	
		18	2A		
		19	3A		
		20	1A		
		21	3A		
		22	1A		
		23	3A		
		24	3A		
		25	2A		
		26	3A		
		27	2A		
		28	3A		
		29	3A	3B	
		30	1A		
		31	3A		
		32	2A		
		33	2A		
		34	2A		
		35	2A	3B	
		36	2A		
		37	2A		
		38	2A		
		39	3A	3B	
		40			

MODEL: REV		CHANGE LIST	MODEL		
			ZR6 MB		
PAGE			FROM	TO	
ZR6 MB	B	Page6:change R175 and R181 to 4.7K for HDMI vender request	1	1A	
	C	Page10:change net name +1.5VSUS_TXLVDS--> +1.8V_TXLVDS	2	1A	
		Page3:Del Q5,Q6,R62,R63	3	1A	
		Page3:change Par Number from AL000780000 to AL000780003 for thermal sensor address change to 9AH	4	1A	
		Page21:Del Q10,Q9,R96,R86	5	2A	
		Page27:R574 stuff and R541 no stuff	6	1A	
		Page31:R300,R301 stuff thermal sensor	7	1A	
		Page37:change PC65,PC67 to 150pF	8	1A	
		Page28:change U2 PartNumber from AL008131001 to AL008131002(LAN chip)	9	3A	
		Page27:change R530,R533 from 10 ohm to 5.1 ohm for headphone	10	3A	
		Page27:change CN8 (usb) 12 pin board to board	11	1A	
		Page26:Change CN5 footprint to cwy027-b0glz-2p-1,CN16(USB)footprint change to usb-c107h6-10405-1-4p-r-v-nb4	12	1A	
		Page30:Change CN7 footprint to 4IN1-R015-212-LM-42P-H-nb4	13	1A	
		Page32:PJ1 footprint change to bat-btj-08qn0b-8p-r-v-nb4	14	3A	
		Page32:Del R510,change Hole15 footprint from h-tc315bc433d106p2 to h-tc315bsd106p2	15	2A	
		Page04:change C493 to no stuff	16	1A	
		Page27:Del T77 and Add R62	17	3A	
		Page26:change Hole21 footprint to h-c236d142pt-8	18	2A	
		Page24:Change D1 `D2 `D3 footprint to led-ht-110nb5-3p	19	3A	
		Page24:Change R218,R234 to shortpad	20	1A	
		Page26:Change R310 to shortpad	21	3A	
		Page10:Change R91,R307,R418,R466,R469 to shortpad	22	1A	
		Page29:Add C466,C467 for EMI,Add R358,R357,R366,R367 and change DGND to LAN GND	23	3A	
		Page26:Add C716 for EMI	24	3A	
		Page30:Change L34 to 0 ohm and C715 to 10P,Change R512,R525,R528,R527 to 20K 1% and Change R526,R515,R524,R522 to 47K 1%	25	2A	
		Page25:Change R1,R4,R10,R365,R369,R368 to 221 ohm and Change D1,D2,D3 part number	26	3A	
		Page14:Change R282 to no stuff	27	2A	
		Page28:Change R26 to no stuff	28	3A	
		Page26:Change Hole29 part number to MBZR6005010	29	3A	
		Page29:Del net name LAN_LNK_LED_PWR	30	1A	
		D	Page14:Add R583 and R315 at GPIO7 for HDMI option,change R583 to no stuff and R315 to stuff	31	3A
			Page24:change HDMI item to no stuff(remove this function)	32	2A
			Page12:change R225,R216,R241,R220,R219,R215,R213,R214,R228,R227 to no stuff for remove HDMI Audio	33	2A
			Page26:Change Hole 16 footprint as hole1	34	2A
		E	Page37:change PR97,PR98 to short-pad ,change PU4 OZ8116 change to OZ8111 for cost issue ,Del PC62	35	2A
			Page27:C670 change value from 1U to 4.7U (CH5471M9907)	36	2A
			Page29:change c478 from 1000p to 220p.(CH122GKI10)	37	2A
			Page28:change C18 from 0.1u to 1000p (CH21006JB10),change C20 from 0.1u to 1u (CH5102K9B06) ,ADD C723 0.1u (CH41002KB93) ,ADD C720 1u (CH5102K9B06)	38	2A
			Page25:change DHP00DA1G03->DHPTME53201	39	3A
			Page24:add C722 (CH6101M9905) to solve ISN issue	40	3B
Page27:the PC beep will change Gain from -6db to -18 db , so R559 needs stuff 10k on all BOM.					
Page34:change PC133 from CC7560JNZ15 to CC7560JNZ02 for cost down					
Page36:change PC139 from CC7560JNZ15 to CC7560JNZ02 for cost down					
Page38:change PC156 from CC7560JNZ15 to CC7560JNZ02 for cost down					
Page33:change PC158,PC162 from CC73301MVB2 to CC73301MZ04 for cost down					
Page37:change PQ6,PQ7 from BAM700200F6 to BAM601K0003 for cost down					
MB Assy' P/N: 31ZR6MB0000/10/20/30/40/50/60/70			Project :ZR6 MB	Document No.:	
Approved by :Andy Chen		Drawing by :Andy Chen	DATE: 2009/03/04		
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